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A Novel High Step-up DC-DC Converter Using State Space Modelling Technique for Battery Storage Applications

Rajanand Patnaik Narasipuram [1,2,*]

[1] Department of Electrical and Electronics Engineering, Vignan's Foundation for Science Technology and Research, Guntur 522213, India

[2] Mobility Group, Eaton India Innovation Center LLP, Pune 411028, India

* Corresponding author. E-mail: rajanand.ee@gmail.com (R.P.N.)

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ABSTRACT: This paper focuses a novel non-isolated coupled inductor based DC-DC converter with excessive VG (voltage gain) is analyzed with a state-space modeling technique. It builds up of using three diodes, three capacitors, an inductor and CI (coupled inductor). The main switch S is turn on due to body diode and voltage stress is reduced at the switch S by using diode D_1 and Capacitor C_1. This paper focuses on design modelling, mathematical calculations and operation principle of DC-DC converter is discussed with state-space modelling technique. The performance has been presented for two different voltages for EV applications, i.e., 12 V, 48 V as input voltages with a high step-up outputs of 66 V and 831.7 V respectively. The converter stability is studied and determined the bode plot along with simulation performance results which are carried out using MATLAB R2022B.

Keywords: DC-DC Converter; Energy Storage System; High Step-Up; State-Space Modelling

1. Introduction

Recently, in every industrial application a boost converter is mostly widely used, due to environmental reaction of utilizing nonrenewable energy and reducing of individual store have complete it mandatory to utilize clean and inexhaustible power sources [1,2]. The application of converter is in energies, PV (photovoltaic), wind and FC (fuelcell) are used as DG systems [3]. These systems be naturally depending on atmosphere. For instance, in some systems, for increasing the output voltage PV cells are united in sequence, the dark effect cannot be obtained in this condition [4]. For boost the output boost converter are used in this system, each PV panels can have controlled itself individually by connecting these converters, with smaller in size along with high conversion gain ratio and greater efficiency are the features of boost converters [5]. For photovoltaic functions, maintaining low current ripples across the input side is also necessary. However traditional boost converter attains required HC (high conversion) ratio with greater D (duty cycle). Moreover, due to less transformation efficiency, reversal-recovery and Electro-magnetic- induction (EMI) troubles, the excess voltage gain will not have achieved [6].

Now a day's, many converter arrangements with various novel techniques has been discussed recently by achieving greater voltage gain and efficiency. There are few techniques which are switched capacitors and voltage lift for getting excess VG [7]. Higher current ripples across the major switch are the significant fault of these converters which reducing the performance effectiveness and voltage increase of the converter [8]. By getting high voltage increase the turns across the coupled inductor is adjusted. However, voltage spikes obtained across main switch because of leakage inductance, and it cause high power dissipation. The storage energy across the leakage inductor should be regained for eliminating such a problem. So, a voltage clamp is needed for such a type of designed converters. Various voltage clamps have been introduced for different coupled inductor-based converters. The major drawback is high input current ripples across the inductor [9]. Due to small effective action of fuel cells, such type of converters is not applicable for these systems. High step up non isolated closed loop coupled inductor base converter has been introduced. By using a greater number of components is the main concern of all these converters, hence this paper discussed about SEPIC based converter has been introduced. The input side current rippled have be reduced due to owning the SEPIC converter has an inductor which is connected at source side [10,11].

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A high step-up CI-based DC-DC power converter shown in Figure 1. As shown in this picture, for reducing input current ripples inductor connected across the input side. Due to C1 and D1 the switching voltage is reduced. This gives a switch S with low on state-resistance Rds_{on} to reduce the conduction losses [12]. However, switching losses are reduced due to ZCS condition. The operation principle explained on given below.

The major contribution of this paper is as followed

1. Proposed a novel DC-DC converter for high gain applications along with mathematical modelling and design parameters.
2. A novel state space modelling technique is presented and analyzed for battery storage applications and EV applications.
3. Detailed simulation model is presented for two different case conditions, case-1 is for 12 V to 66 V conversion with a $D = 0.5$, where in case-2 48 V to 831.7 V conversion with a $D = 0.7$.

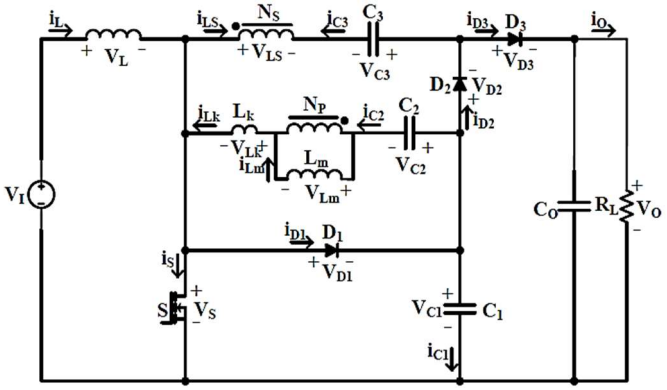
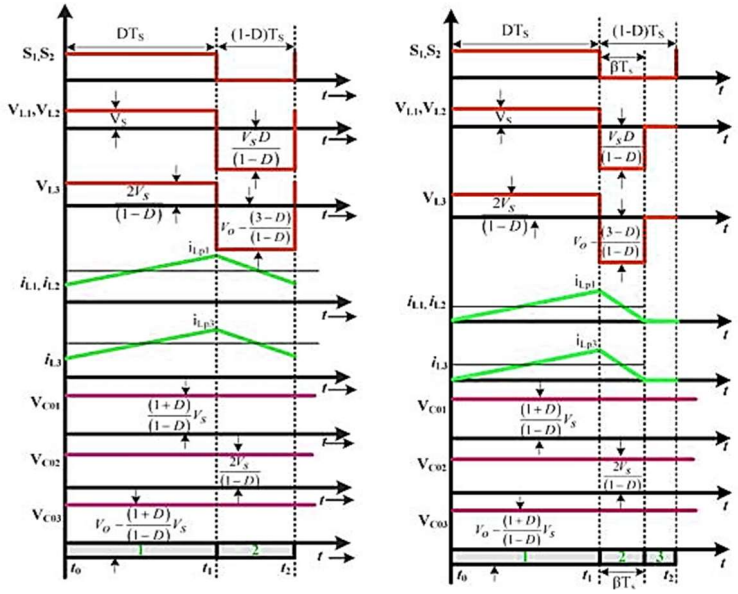


Figure 1. Non-Isolated HG DC-DC converter.

2. Operating Principle of the Non-Isolated CI DC-DC Converter

The operating principle and analysis of the closed loop DC-DC converter, during this entire derivation there are some ideal conditions to be consider. All capacitors and inductors are having the minimal voltage ripples and current ripples which are coming under 2% [13]. The continuous and discontinuous conduction mode waveforms are presented in Figure 2.



(**a**) CCM Mode (**b**) DCM Mode

Figure 2. Ideal waveforms for Proposed DC-DC converter: (**a**) CCM; (**b**) DCM.

2.1. Analysis of CCM for Proposed DC-DC Converter

The main non-isolated DC-DC converter operation analyzed under CCM at single switching period consisting of five different time intervals. The current direction in the main converter and waveforms is shown in Figure 3. The inductor current of the non-isolated CI is defined in Equation 1:

$$i_{Ls=}\frac{i_{Lm}-i_{Lk}}{n} \quad (1)$$

The inductor current and secondary sided non-isolated coupled inductor current cannot change synchronously. The complete operation and steady-state study of the non-isolated converter is discuss on below.

2.1.1. Mode I [$t_0 < t < t_1$]

The main switch S and Diode D3 is turned on. i_{Lk} is increased to equal i_{Lm} in this time interval. This mode ends when the i_{Lk} & i_{Lm} of the non-isolated coupled inductor are the same.

The equation of i_{Lk} can be written as:

$$i_{Lk} = \frac{1}{L_K}\int_{t_0}^{t_1}\left(V_{C1} - V_{C2} + \frac{V_0 - V_{C3}}{n}\right)\mathrm{d}t \tag{2}$$

First mode of interval is very small and the V_{LK} is high, and the value of L_K is less. By the V_1 the inductor L is magnetized. After completed this time interval, the N_S current of the non-isolated coupled inductor as well as a result, the diode i_{D3} becomes to zero. Using KCL, the i_S can be written as:

$$i_s = i_L + i_{Lk} - i_{Ls} \tag{3}$$

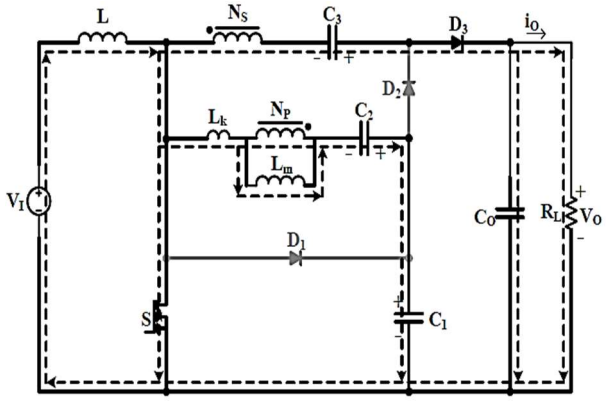


Figure 3. Interval [t_0-t_1] in Mode-1.

2.1.2. Mode II [$t_1 < t < t_2$]

The switch is quiet on in this time interval and the circuit mode is shown in Figure 4. The i_{Lm} decreases linearly and exceed i_{LK}. The i_{LK} equation can be taken as follows:

$$V_{Lk2} = \frac{\left(i_{Lk(t2)} - i_{Lk(t1)}\right)}{DT_S}L_K, \quad i_{Lk} = ni_{D2} + i_{Lm} \tag{4}$$

The diode D_2 turns on due to flow of N_S current. Thus, Diode D_2 current increase gradually from zero. The C_3 is Energized Due to the N_S current of the non-isolated coupled inductor The stored power in capacitor C_1 is de-energized to the capacitor C_2 and coupled inductor. Due to the input power supply the inductor L is magnetized. This time interval completed when switch is in open circuited. In this time interval, by using KVL, the voltage equation can be obtained as follows

$$V_L = V_1 \tag{5}$$

$$V_{Lm} = V_{C2} - V_{C1} - V_{Lk2} \tag{6}$$

$$V_{C3} = (n+1)V_{C1} - nV_{C2} - nV_{Lk2} \tag{7}$$

where $n = NS/NP$

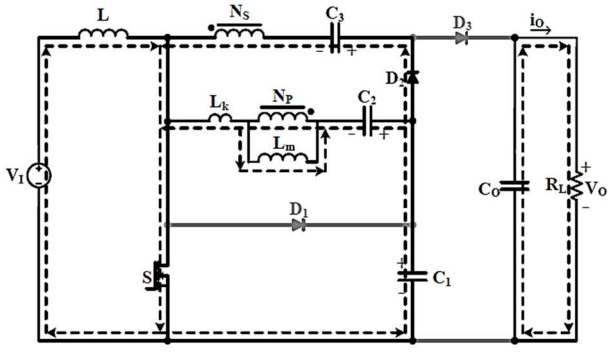


Figure 4. Interval [t_1-t_2] in Mode-2.

2.1.3. Mode III [$t_2 < t < t_3$]

The inductor current i_L discharge through diode D_1 and it turns on similarly the switch is open circuited at this time interval and shown in Figure 5. The D_1 and D_2 currents are written as:

$$i_{D1} = i_L + i_{Lk} + i_{D2} \tag{8}$$

$$i_{D2} = \frac{i_{Lk} - i_{Lm}}{n} \tag{9}$$

The i_{Lk} is de-magnetized continuously and its equals the i_{Lm}. The i_{D2} remains zero at this time interval. i_{LK} can be written as follows:

$$i_{Lk} = \frac{1}{L_k}\int_{t_0}^{t_1}\left(\frac{V_{C3}}{n} - V_{C2}\right)\mathrm{d}t \tag{10}$$

From above equation, a low value of leakage inductor and a high negative voltage creates its current slope to be high and it also present at small time interval. Due to the input source energy and de-magnetizing inductor L the capacitor C_1 is charged [13–16]. When diode D_2 is tuned off then this mode will be ends.

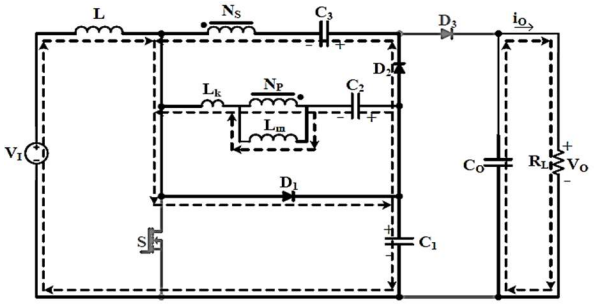


Figure 5. Interval [t_2-t_3] in Mode-3.

2.1.4. Mode IV [$t_3 < t < t_4$]

Due to V_1 and Inductor storage energy the capacitor C_1 is charged in this time interval and shown in Figure 6. In this mode, the leakage inductor voltage will be altered. Its voltage equation will be able to taken as follows:

$$V_{Lk4} = \frac{\left(i_{Lk(t4)} - i_{Lk(t3)}\right)}{d_4 T_S} L_K, \quad i_{Lk} = -n i_{D3} + i_{Lm} \tag{11}$$

d_4T_S are time interval of this mode. Due to the N_S current of the non-isolated coupled inductor the C_0 is charged. The diode current D_1 will be written as:

$$i_{D1} = i_L + i_{Lm} - (n+1) i_{D3} \tag{12}$$

when i_{D1} becomes zero then this mode will be ends. However, the slope of i_{Lm} is less than i_{LK}, according to equation (1), the slop i_{D3} is +ve. In this mode the V_L, $V_{Lm,}$ can be written as:

$$V_L = V_1 - V_{C1} \tag{13}$$

$$V_{Lm} = -V_{C1} - V_{Lk4} \tag{14}$$

$$V_{Lm} = V_{C1} + V_{C3} + nV_{C2} + nV_{Lk4} \tag{15}$$

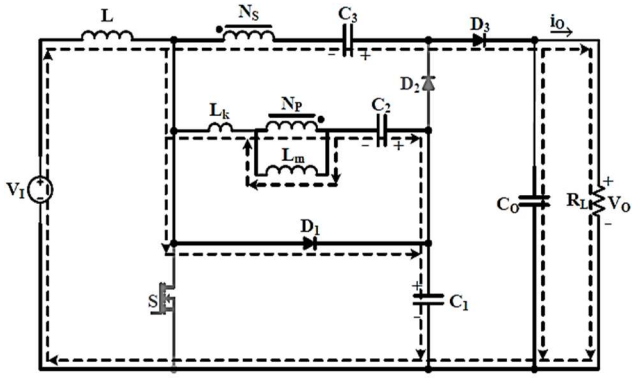


Figure 6. Interval [t_3-t_4] in Mode 4.

2.1.5. Mode V [$t_4 < t < t_5$]

Diode D_3 is still on in this mode. Due to i_{D3} the C_0 is energized. The i_{D3} written as:

$$i_{D3} = \frac{i_L + i_{Lm}}{n+1}, i_{Lk} = \frac{-n}{n+1}\left(i_L - \frac{i_{Lm}}{n}\right) \tag{16}$$

The diode D_3 and the i_{LK} slope calculate on the i_L, i_{LM} slope. Eliminating the i_L, i_{Lm} ripples taking the slope of i_{D3} and the i_{LK} becomes to zero. Then V_{Lk} will be zero. As stated in this equation, current is zero when S becomes on at the starting of mode one and shown in Figure 7. So, under zero current the switch is short circuited. Using KVL the voltage equations be able to be taken as follows:

$$V_{Lm} = -V_{C2} - \frac{n}{n+1}V_{Lk4} - \frac{V_{Lk5}}{n+1} \tag{17}$$

$$V_L = V_1 - V_{C1} - \frac{n}{n+1}(V_{Lk4} - V_{Lk5}) \tag{18}$$

The slope of i_{Lk} in modes 2 & 4 can be used to calculate V_{LK2} & V_{LK4}. The non-isolated coupled inductor primary and secondary sides are in series with the capacitors C_2 and C_3, i_{Lk} and i_{Lm} avg. currents are zero, according to Amp-Sec balance principle. By applying balancing formulas on the C_1, C_2 &C_3, C_0 it can be justified that the i_o equal to the average value of diode current. Therefore, the following equation can be obtained from Figure 2,

$$\langle i_{D2} \rangle = I_0 \Rightarrow D i_{D2\,peak} = 2I_0 \Rightarrow i_{D2\,peak} = \frac{2I_0}{D} \tag{19}$$

$$\frac{i_{Lk} - i_{Lm}}{n} = i_{D2\,peak} = \frac{2I_0}{D} \Rightarrow i_{Lk\,peak} = \frac{2nI_0}{D} \tag{20}$$

So the $i_{ripples}$ of the L and L_m are also in-considered in voltage gain computation. The i_{stress} of the S and D_1 can be obtained as given below:

$$i_{D1peak} = i_L + i_{Lm} + (n+1)i_{D2peak} = \left(\frac{2n+2-nD}{D(1-D)}\right) I_0 \tag{21}$$

By in-considering the 3rd mode using this equation, the 4th time period can be obtained as

$$\langle i_{D1} \rangle = I_0 = \frac{d_4 T_S I_L}{2T_S} \Rightarrow d_4 = \frac{2(1-D)}{n+2} \tag{22}$$

Due to (4) and (19) equations The voltage V_{Lk2} can be found as:

$$V_{Lk2} = \frac{2nV_0}{D^2} Q, Q = \frac{f_S L_K}{R_L} \tag{23}$$

where, f_{switch} and R_L, respectively. Join Volt-Sec balance basis on the L_K. By neglecting mode 1 and 3, the following equation is obtained.

$$DT_S V_{LK2} + d_4 T_S V_{LK4} + 0 = 0 \Rightarrow V_{Lk2} = -\frac{d_4}{D} V_{Lk4} \tag{24}$$

Applying Volt-Sec balance basis on the inductors the output is:

$$V_{C1} = \frac{V_1}{(1-D)} - \frac{n^2}{(n+1)(n+2)} V_{Lk4} \tag{25}$$

$$V_{C2} = \frac{DV_1}{(1-D)} - \frac{n^2}{(n+1)(n+2)} V_{Lk4} \tag{26}$$

$$V_{C3} = \frac{1+n-nD}{(1-D)} V_1 - \frac{n^2}{(n+1)(n+2)} V_{Lk4} - nV_{Lk2} \tag{27}$$

$$M = \frac{(n+1)(1-D)D^2}{(n+1)(1+D)D^2 - n^2(-2(1+n)+nD) \times Q} \left[\frac{2+n}{1-D}\right] \tag{28}$$

The V_{gain} of proposed converter is

$$M_{CCM} = \frac{2+n}{1-D} \tag{29}$$

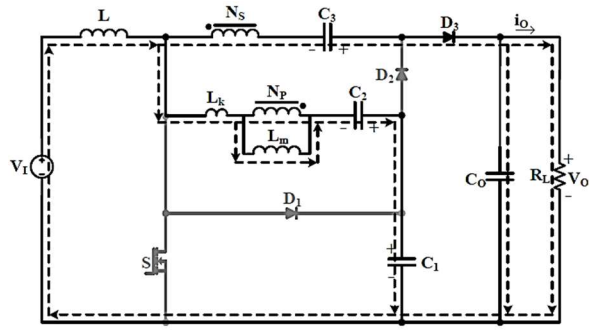


Figure 7. Interval [t_5-t_6] in Mode-5.

The voltage stresses of the switches/diodes can be formulated According to the operation principle of the new converter. To find the relevant semiconductors of the non-isolated DC-DC converter, the V_{Stress} & i_{Stress} should be obtained.

$$V_S = V_{D1} = V_{C1} = \frac{V_1}{1-D} \tag{30}$$

$$V_{D2} = V_{D3} = V_0 - V_{C2} = \frac{(n+1)V_1}{1-D} \tag{31}$$

From equation (19) the $D_{2(peak)}$ is obtained. The value of S_{peak} and diode $D_{1(peak)}$ currents is as follows:

$$i_{s\,peak} = i_{D1\,peak} = \left(\frac{2n+2-nD}{D(1-D)}\right) I_0 + \left(\frac{1}{L} + \frac{n}{L_m}\right)\frac{DV_1}{2f_s} \tag{32}$$

Based on Figure 3 and taking equation (32), the current value of $D_{3(peak)}$ can be explained as given below:

$$\langle i_{D3} \rangle = I_0 = \frac{i_{D3\,peak}(2(1-D)-d_4)}{2} \Rightarrow i_{D3\,peak} = \frac{(n+2)I_0}{(n+1)(1-D)} \tag{33}$$

By neglecting the ESR of the C_0, the V_0 ripple of the new converter can be given as follow

$$V_{C0}(DT_S) = V_{C0}(0) + \frac{1}{C_0}\int_0^{DT_S} i_{c0}(t)dt \Rightarrow |\Delta V_{C0}| = \frac{DV_0}{f_s R_L C_0} \tag{34}$$

$$\Delta V_{C_0}^{ESR} = r_{c_0}\,\Delta i_{c_{0\,max}} \Rightarrow \Delta V_{C_0}^{ESR} = r_{c_0}\left(\frac{(n+2)V_0}{R_L(n+1)(1-D)}\right) \tag{35}$$

3. Controller Design and Stability Performance

This section deals with the proposed state-space modelling technique to analyses the converter dynamic conditions [14]. The control technique is derived from the input to output with respective to control the output of the converter and the transfer functions are derived as mentioned in the below. The inductors and capacitors are connected in parallel, hence all the components are named and derived as L, C using second order transfer function [15].

Equations (36) and (37) denote the input to output relation and control to output transfer function, the frequency plots are drawn using the same equations and by using the original values the derived equations are in (38) and (39) respectively [16]. Figure 8 denotes the frequency response plots of the system with proposed system.

$$\frac{\widetilde{V_o(s)}}{\widetilde{V_g(s)}} = \frac{R_o(1+2D)(1-D)}{3LC_oR_os^2+3Ls+(1-D)^2R_o} \tag{36}$$

$$\frac{\widetilde{V_o(s)}}{\widetilde{d(s)}} = \frac{[(1+2D)(1-D)V_g - 3LCI_os]\left(\frac{R_o}{(1-D)}\right)}{3LC_oR_os^2+3Ls+(1-D)^2R_o} \tag{37}$$

$$\frac{\widetilde{V_o(s)}}{\widetilde{V_g(s)}} = \frac{217.5}{2.6e^{-6}s^2+3e^{-4}s^2+21.75} \tag{38}$$

$$\frac{\widetilde{V_o(s)}}{\widetilde{d(s)}} = \frac{2088-0.03966s}{2.6e^{-6}s^2+3e^{-4}s^2+21.75} \tag{39}$$

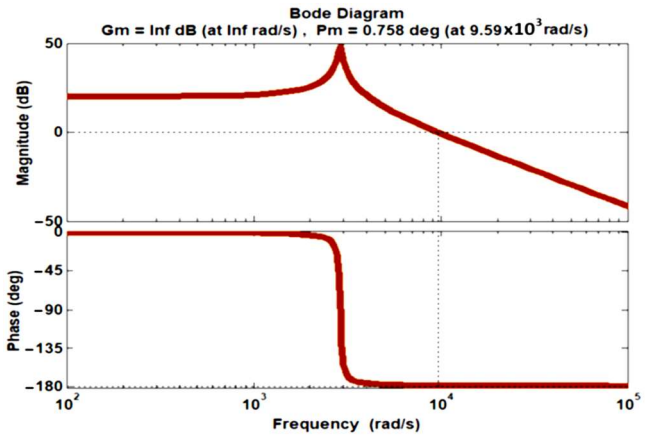


Figure 8. Bode Plot Stability Analysis.

4. Simulation Results

This section gives a brief on simulation results and the performance analysis of proposed DC-DC converter for battery storage system application is presented in two different conditions. In the first condition converter is designed at a duty cycle of 0.5 with an input and output voltage parameters are showed in Table 1. In the second condition converter is designed at a duty cycle of 0.7 at different voltage conditions and parameters are showed in Table 1.

Table 1. Proposed Circuit Parameters.

Parameters	Electrical Values
Input Voltage	12 V, 48 V
Output Voltage	66 V, 831.7 V
Capacitors $C_{1, 2, 3, 4}$	47 µF
Filter Capacitor C_0	180 µF
Inductors	365 µH
Couple-Inductor L_m	125 µH
Switching Frequency	35 kHz

Figure 9 shows the condition 1, where the converter is operating at in input voltage of 12 V at an output voltage of 48 V at a duty cycle of 0.5, and the other associated waveforms of switch voltage, diode voltage and capacitor voltage are presented. In Figure 10 the current waveforms of associated components like output current, inductor currents and diode currents are presented. From Figure 11 it illustrates the converter condition 2, which explains the converter adaptability at high voltage conversion from 48 V to 831.7 V along with switching voltage.

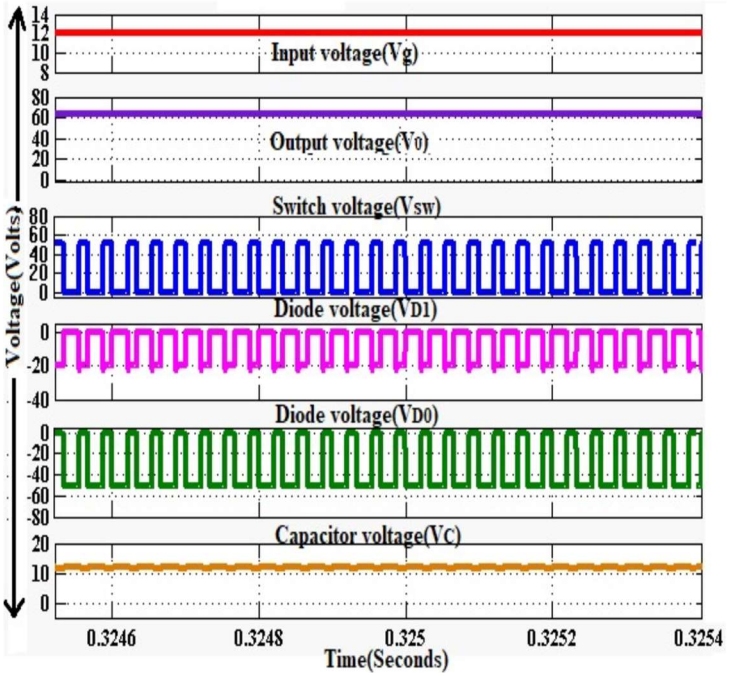


Figure 9. Voltage Profile of Proposed DC-DC Converter.

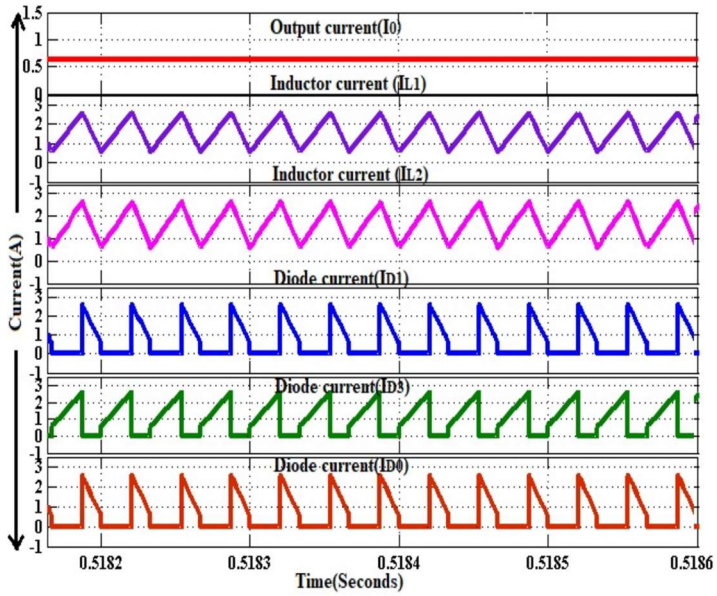


Figure 10. Current Profile of Proposed DC-DC Converter.

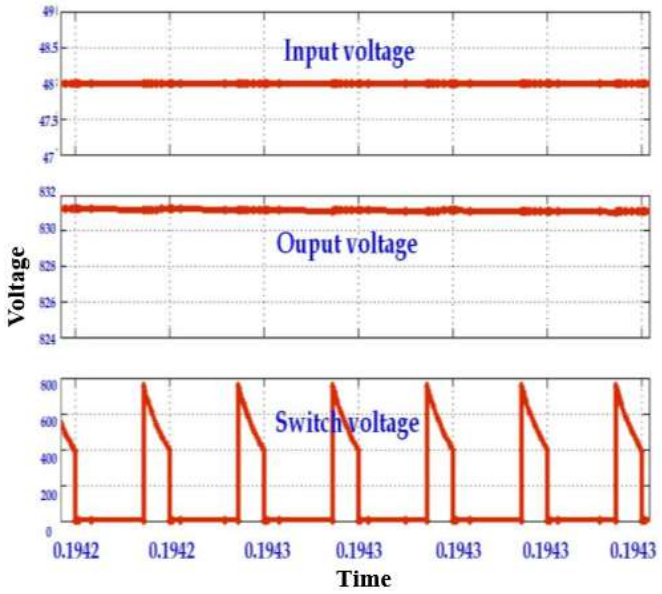


Figure 11. At Different Voltage of Input and Output with $D = 0.7$.

6. Conclusions

A novel closed loop high step-up DC-DC converter with state-space controller for boost applications with stiff voltage regulation is presented in this paper. The new converter had major advantages like high voltage gain, low current ripples at input side and zero current switching, low V_{stress} at switch. The converter simulations are presented at two different conditions of duty cycles which is at $D = 0.5$ and 0.7. At all these conditions the converter is performed well and can be used as battery charger as well as auxiliary DC-DC converter for vehicle applications as well as PV systems.

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Ethics Statement

Not applicable.

Informed Consent Statement

Not applicable.

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Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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