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Review

Review of Gallium Nitride Devices and Integrated Circuits at High Temperatures

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ABSTRACT: In various industrial applications, including aviation, electric vehicles, and drilling, the demand for semiconductor devices and associated circuits with high thermal stability is progressively increasing. Wide-bandgap semiconductor Gallium Nitride (GaN) devices exhibit the advantages of fast switching capability, low on-resistance, and the ability to operate at high temperatures. These advantages have made them potential candidates for integrated circuits in high-temperature environments in recent years. Lateral GaN devices promote monolithic integration, which consequently increases power density and reduces cost of cooling systems. Hence, it is worthwhile to investigate the performance of GaN devices in high-temperature environments. This review aims to present a thorough review of high-temperature characteristics of GaN devices and integrated circuits. The performance of GaN devices at high temperatures, such as threshold voltage，saturation current and on-resistance, has been reviewed in response to different structures. The underlying degradation mechanisms related to the intrinsic properties of structures and fabrication technology are discussed at high temperatures. The thermal performance of GaN small signal integrated circuits and power converters was presented. This paper systematically examines the advantages and challenges of GaN devices and integrated circuits at high temperature environments.

Keywords: Gallium nitride; High temperature; Integrated circuits; Thermal degradation

1. Introduction

Integrated circuits play a vital role in diverse industries and serve as the foundation of the modern information society. The majority of commercial integrated circuits are based on silicon devices. However, the performance of silicon devices significantly declines at elevated temperatures, and they may even become damaged when the operating temperature exceeds 125 ℃. Numerous industrial applications require high-temperature capabilities that exceed 125 ℃, even 500 ℃. For instance, turbine engines necessitate the placement of sensors in an ambient temperature of 500 ℃ [1]. Similarly, in aerospace exploration, electronic components are required to withstand extreme radiation environments and ambient temperatures that can surpass 500 ℃ [2]. The application of integrated circuits in numerous scenarios, such as aerospace, will be restricted. Extra cooling systems can mitigate this issue, but it hinder the enhancement of integration and increase the volume and cost of the integrated circuits. Consequently, it is imperative to explore alternative approaches that are more integration-friendly. Wide bandgap semiconductors, such as gallium nitride (GaN) and Silicon carbide (SiC), are considered promising candidates for applications necessitating exposure to elevated temperatures. SiC and GaN are well-established wide bandgap devices known for their attractive features, including high current carrying capabilities, low on-resistances, wide bandgap, high breakdown field and good thermal conductivity [3]. Meanwhile, the combined figure of merit (CFOM) of GaN devices based on various substrates was evaluated, and it was observed that the GaN device utilizing a sapphire substrate exhibited the highest CFOM [3].

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Compared to Si-based devices, a proposed GaN vertical superjunction high electron mobility transistor (SJ HEMT) exhibits substantial performance improvement with respect to on-state resistance and breakdown field [4]. Furthermore, HEMTs can show stable DC characteristics after being tested at 400 ℃ for 25 h, which is manifested by negligible changes in characteristics such as saturation current and threshold voltage. Reviews have been published on the relevant characteristics of wide bandgap devices, including the advantages and challenges [5–8]. Additionally, specific review [9,10] concentrated on furnishing background information about GaN power devices and GaN-based integrated circuits. The existing reviews cover the high-temperature device characteristics of HEMTs and some basic HEMT-based circuits and sensors [11].This review aims to analyze thermal degradation mechanisms and high-temperature applications of GaN HEMTs from a process perspective. The paper lists the manufacturing processes and their high-temperature limits associated with different device structures. It then comprehensively analyzes the results based on theoretical models, simulation data, and experimental results. Subsequently, from an application perspective, this review outlines various GaN integrated circuits and analyzes the performance degradation at high temperatures. Numerous studies have demonstrated that GaN integrated circuits exhibit exceptional thermal stability at temperatures ranging from 200 ℃ to 400 ℃. This review offers valuable insights for small power devices and their integrated circuit applications.

This review presents the performance of GaN devices in Section 2, including the basic principles of GaN devices. This section also examines the high-temperature performance of various GaN devices and explains the effect of temperature on their fundamental properties. In Section 3, the degradation mechanisms under high temperatures are introduced. Moreover, the integrated circuits based on GaN technologies are examined in Section 4. Section 5 summarises our main findings.

2. Gallium Nitride Devices

Previous research indicated that GaN, a wide bandgap semiconductor, is a promising material choice for high-temperature environments. This section will examine GaN devices proposed and applied at high temperatures, including their characteristics and similarities.

GaN HEMTs can be categorised into two types: enhancement mode (E-mode) and depletion mode (D-mode). Different gate process techniques have been implemented in GaN HEMTs, such as metal-insulator-semiconductor (MIS) HEMTs, P-type GaN HEMTs, *etc.* The effect of temperature on the electrical properties of GaN devices has been reported. GaN devices could operate at a high temperature of up to 600 ℃, indicating their great potential for high temperature applications.

The heterostructure of Aluminium Gallium Nitride (AlGaN) and GaN is proposed to replace Si MOSFETs for high frequency power switching applications. However, the natural channel of this heterojunction makes it a normally-on device. Normally-off AlGaN/GaN HEMTs with positive gate threshold voltage are recommended for power supply applications to ensure safe operation. E-mode devices can be achieved by three technical approaches: p-GaN (or p-AlGaN) cap layers, gate recess, and fluorine plasma processing.

2.1. The HT Characteristics of GaN HEMTs

The performance of GaN devices significantly affects the performance of circuits in power electronics, making the study of device characteristics at different temperatures a valuable area for further research. The manufacturing technology of E-mode GaN HEMTs by fluorine implantation has attracted significant interest [12,13]. The principle of F implantation is to introduce negative fluorine ions in the AlGaN barrier, resulting in the effective depletion of the 2DEG in the channel.

In 2007, a normally-off GaN HEMT with fluorine plasma treatment was fabricated and measured in a temperature range from 25–375 ℃ [12]. The E-mode AlGaN/GaN HEMT has a threshold voltage (V_{th}) of 0.76 V at 23 ℃, and the drain current at V_{gs} =3 V is 250 mA/mm, with a peak transconductance of 120 mS/mm. As the measurement temperature increases, threshold voltage, drain current density, and peak transconductance are 0.24 V, 56 mA/mm, and 29 mS/mm at 375 ℃, respectively. As summarized in Figure 1, the D-mode device shows a negative threshold voltage shift of 0.18 V at 375 ℃ compared to the E-mode device. A decrease in current density and peak transconductance was observed as 87 mS/mm, 267 mA/mm at V_G = 1 V, respectively.

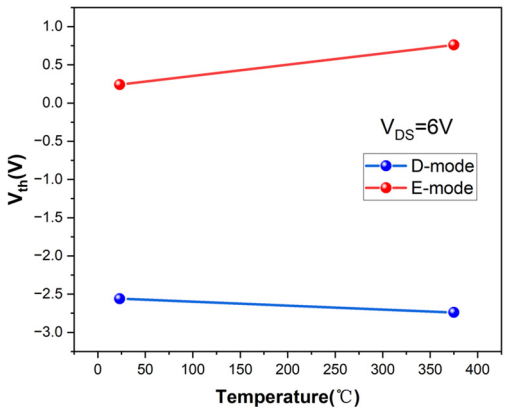


Figure 1. Characteristics of D-mode HEMTs and E-mode HEMTs at different temperatures (created by the authors based on [12]).

Based on Fluorine ion treatment, post-gate annealing technology for GaN HEMTs can increase the threshold voltage at room temperature and reduce voltage threshold drift at high temperatures [13]. As temperature increases, the negative shift of the threshold voltage is caused by thermal excitement of electrons which are trapped by Fluoride ions. Consequently, the amount of negatively charged Fluoride ions in the AlGaN layer decreases, resulting in a negative shift of the threshold voltage at high temperatures. The negative temperature coefficient of V_{th} in Fluorine ion-based HEMTs can be alleviated by a thinner barrier and slightly lower Al compositions, while the increased threshold voltage can be achieved by larger doses of plasma treatment [14].

The leakage current of GaN HEMTs increases with rising temperature. However, the increased magnitude of leakage current in E-mode devices is significantly lower than that of D-mode devices, as illustrated in Figure 2. The difference is due to the presence of fluoride ions in the AlGaN layer of HEMTs [15]. The threshold voltage has a small variation across various temperatures. The on-state resistance (Ron) of GaN devices also increases as the temperature rises. The primary causes are high off-state voltage and switching transients at elevated junction temperatures [16].

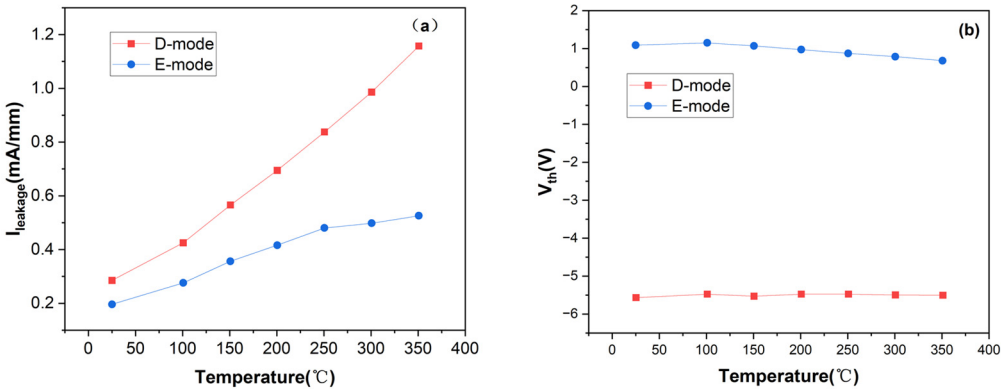


Figure 2. The temperature dependence of off-state drain leakage current (I_{leak}) (**a**) and V_{th} (**b**) for E/D-mode GaN HEMTs by the planar process (created by the authors based on [15]).

Studies demonstrate that employing a high-thermal-conductivity substrate, particularly SiC, can reduce the effective thermal resistance by an order of magnitude and significantly enhance the thermal performance of GaN devices. Gaska et al. [17] were the first to fabricate AlGaN/GaN HFETs on a 6H-SiC substrate, achieving a room-temperature dissipated power of 0.6 MW/cm² and stable operation up to 300 °C, verifying that GaN-on-SiC boosts DC power handling to over three times that of sapphire substrate based devices. Maeda et al. [18] subsequently pushed the operating temperature to 400 °C on SiC substrates, with only an 8% drop in transconductance. This demonstrated that the high thermal conductivity substrate effectively suppresses the rise in junction temperature. In 2002, Arulkumaran et al. [19] compared AlGaN/GaN HEMTs and found that device performance on a SiC substrate outperformed that on a sapphire substrate when the temperature is less than 300 °C. Cuerdo et al. [20] later used source/drain resistance extraction to show that Si (111) devices, owing to higher thermal conductivity, exhibit higher I_D and G_m than sapphire at room temperature. However, this difference disappears above 300 °C, reinforcing SiC's advantages in the typical operating

range. Islam et al. [21] further demonstrated that combining SiC with 140 nm short-gate structures retains 35% of the initial current at 500 °C, whereas sapphire substrates show faster degradation, underscoring SiC's superior heat dissipation.

2.2. The HT Characteristics of GaN MIS-HEMTs

GaN devices often incorporate gate insulators under the gate electrode to improve device performance, such as reducing leakage current and increasing gate swing. Alumina (Al_2O_3) functions as a metal insulator, thereby preventing gate metal sinking at elevated temperatures and reducing leakage current. This effect is evident in the fact that metal insulators can withstand temperatures in excess of 600 °C without degradation, whereas HEMTs can only tolerate temperatures up to 300 °C before experiencing a sudden increase in leakage current [22]. The DC characteristics at HTs are shown in Figure 3.

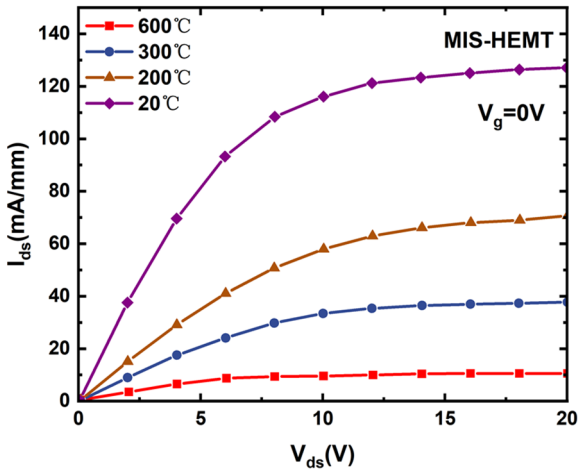


Figure 3. DC characteristics of GaN MIS-HEMT at high temperatures (created by the authors based on [22]).

A GaN MIS-HEMT using aluminum oxide as the gate dielectric was measured from 25 °C to 600 °C. The results indicates that the R_{on} of the MIS-HEMT increased by about eight times [22]. Furthermore, the gate dielectric can be achieved through multilayer fluorinated ALD-Al_2O_3 layers, which would lead to a high threshold voltage at room temperature, while the threshold voltage presents a slight negative shift under elevated temperatures, which is affected by the thickness of the barrier layer [23,24]. AlGaN barrier recess technology with different etching depths has different impacts on GaN devices shown in Figure 4. GaN MIS-FETs fabricated with fully recessed gate technology can yield a beneficially greater V_{th}, thus reducing the likelihood of false turn-on events. The V_{th} of partially recessed MIS-HEMTs and fully recessed MIS-FETs are +0.4 V and +2.37 V at room temperature, respectively. When the temperature reaches 200 °C, the threshold voltage shift ΔV_{th} is −0.76 V and −0.21 V for the partially and fully recessed devices, respectively. However, on-state resistance is negatively affected by the removal of the heterojunction in Figure 4b, resulting in a relatively high R_{on} (13.2 Ω·mm). The partially recessed MIS-HEMT in Figure 4a maintains a thin barrier layer, leading to a smaller R_{on} of 9.6 Ω·mm [25].

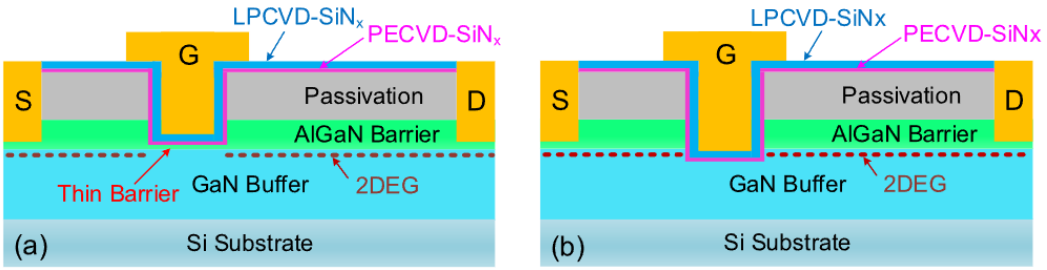


Figure 4. (**a**) MIS-HEMT with partially recessed-gate structure and (**b**) MIS-FET with fully recessed-gate structure [25].

Combined with fluorine plasma implantation and gate recess technology, Liu et al. [26] designed an E-mode MIS-HEMT, as illustrated in Figure 5. This hybrid structure leads to a less negative V_{th} shift than MIS-HEMTs without gate recess. The device presents a slight negative V_{th} shift of -0.5V from room temperature to 200 °C [26]. The experimental results indicate that the V_{th} thermal stability of the E-mode device is improved as the barrier thickness is reduced.

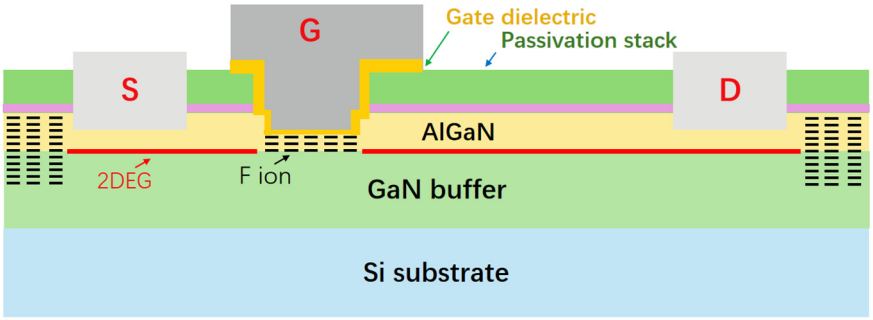


Figure 5. Schematic cross-section of the hybrid E-mode MIS-HEMT (created by the authors based on [26]).

Wang et al. [24] used the charge analytical model and Poole-Frenkel trap emission theory to study the fluorinated trap states distribution of GaN MIS-HEMTs. The positive correlation between the fluorine treatment power and the trap state density is clarified. An improved DC Extraction method [27,28] based on the UFM model proposed by Dasari et al. yields a series of parameters that consider factors such as self-heating effects in GaN HEMTs. In subsequent work [29], they used this method to study the temperature dependence and high-temperature characteristics of low field channel mobility μ_0 and parasitic resistances R_S/R_D. Figure 6 shows the parameters extracted by this model, where mobility μ_0 decreases with increasing temperature, while 2DEG resistance increases. All the variations follow a power law $\sim T^{\gamma}$ ($-3.42 < \gamma < -2.18$).

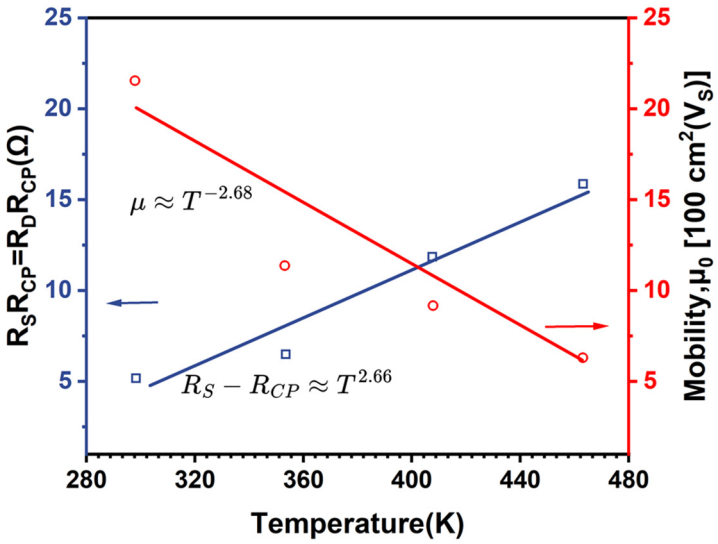


Figure 6. Temperature dependence of μ_0, ungated 2-DEG resistance $R_{S-}R_{CP} = R_D - R_{CP}$ at $V_{GS} = -4$V and μ_{s0} (created by the authors based on [29]).

The IV models of GaN HEMTs include empirical models, semi-empirical models, *etc.* [30–34]. Figure 7 shows high-temperature I_D-V_{GS} prediction curves of HEMTs based on a semi-empirical model [35] and the experimental verification results, indicating good agreement. By integrating this model into the temperature simulator [36], the high-temperature failure mechanism of GaN HEMTs was found to be related to the drain-gate leakage current associated with the Schottky gate.

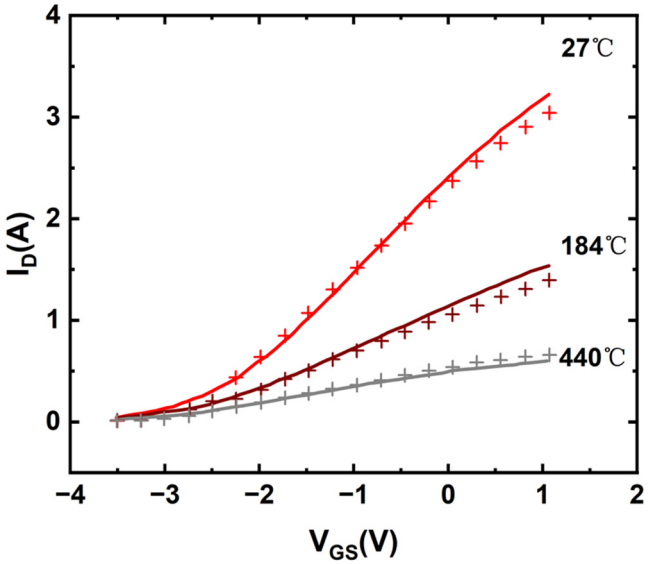


Figure 7. Model validation for high temperatures up to 440 °C. Simulated (lines) versus measured transfer characteristics (symbols) (created by the authors based on [35]).

Time Dependent Dielectric Breakdown (TDDB) is one of the important tests to evaluate the reliability of power devices. Warnock [37] investigated the temperature dependence of TDDB in GaN MIS-HEMTs and found that both t_{1BD}(time-to-first breakdown) and t_{HBD}(time-to-hard breakdown) significantly decrease as the temperature increases to 150 °C. In another study [38], when the MIS-HEMT was in the Progressive Breakdown(PBD) stage, I_G exhibited a power-law dependence and a temperature dependence under negative gate bias, along with dual-exponential behavior at high temperatures, such as 125 °C.

2.3. The HT Characteristics of P-GaN HEMTs

Liu et al. [39] proposed a p-GaN gated AlGaN/GaN HEMTs with HR-GaN layers that can suppress a positive shift at 500 K, as illustrated in Figure 8. Clément et al. [40] studied the impact of temperature on the performance of p-GaN HEMTs on Si and SiC substrates. When the temperature increases from 20 °C to 420 °C, the saturation current decreases by 70%, and R_{on} increases by approximately five times. The results indicate that the different substrates and doping hardly effect the threshold voltage change. Above 200 °C, the temperature-dependent threshold is around $\Delta = 0.125$ mV/°C. In p-GaN gate HEMTs, V_{th} shift is mainly caused by the interface state of p-GaN layer and the GaN buffer at high temperatures. R_{on} increases and g_m decreases due to the degradation of electron mobility at high temperatures.

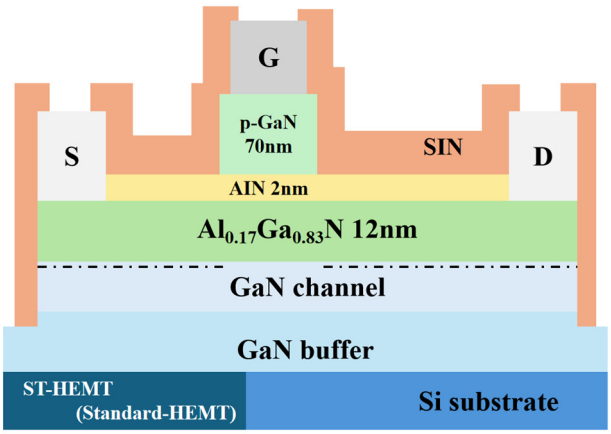


Figure 8. The representative cross-section diagram of the p-GaN HEMT structure (created by the authors based on [39]).

Reference [41] reported the degradation behaviour and physical mechanism of the AlGaN/GaN HEMTs with a p-GaN gate after High-Temperature Gate Bias (HTGB) stress at 150 °C. The results indicate that the threshold voltage and gate leakage current experienced a significant increase, while the saturation current obviously decreased after the HTGB stress. However, the on-state resistance and reverse characteristics remained unchanged. Similar gate

degradation mechanisms were reported in reference [42], which proposed that both the gate breakdown voltage (BV) and mean-time-to-failure (MTTF) exhibit a positive temperature dependence.

Zhang et al. [43] proposed a novel Surface Reinforcement Layer (SRL) technology. Time-Dependent Gate Breakdown (TDGB) tests performed on p-GaN HEMTs at 150 °C demonstrated a higher maximum applicable gate voltage $V_{G\text{-}max}$ and could sustain a higher gate current I_G, thereby significantly enhancing high-temperature gate reliability. This advancement paves the way for the development of more reliable p-GaN gate power devices. Meanwhile, Millesimo et al. [44] analyzed the TDGB test in p-GaN HEMTs at high temperatures. Their work focused on investigating the impact of different isolation processes on long-term gate reliability. It revealed two distinct failure mechanisms (area-related and isolation-related) with a complex interplay between temperature and gate bias.

2.4. Other Structures of GaN Devices

In addition to conventional GaN MIS-HEMTs, some novel GaN devices are designed to facilitate the advancement of power electronics circuits under extreme thermal conditions. By positioning a floating ohmic electrode between the source and gate of the device for current sensing, as shown in Figure 9. It demonstrates a favourable current sensing ratio at temperatures ranging from 25 ℃ to 160 ℃ [45].

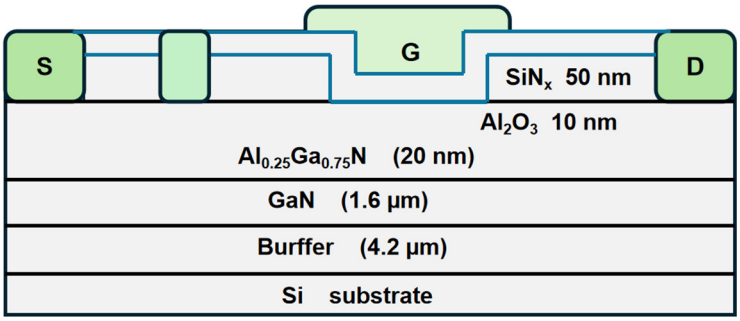


Figure 9. Schematic cross-section of the MIS-HEMT with a current sensor (created by the authors based on [45]).

Compared to the lateral GaN HEMT, the vertical GaN Fin-JFET in Figure 10 presents some advantages, such as a higher breakdown voltage (BV) of 1.2 kV, greater current conduction capability, excellent heat dissipation capability, and lower on-resistance drift rate [46]. However, a drawback of this device is that it is challenging to be monolithically integrated, which would limit the application range.

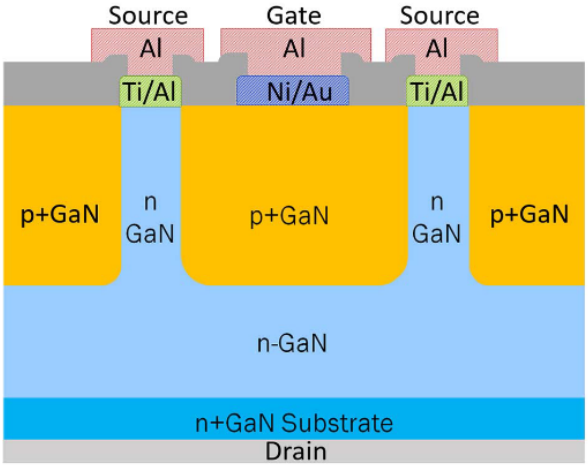


Figure 10. Schematic cross-section of the fabricated vertical GaN Fin-JFET [46].

Another GaN PIN diode structure is shown in Figure 11 [47]. The Ron of this kind of diode structure is found to become unstable under the thermal stress of 400 ℃ for a long time, which provides a reference for the reliability study of GaN vertical devices.

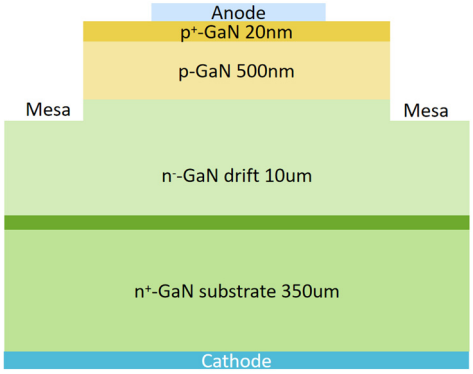


Figure 11. Schematic cross-section of the GaN PIN diode (created by the authors based on [47]).

Figure 12 is the schematic cross-section of a GaN MOS-HEMT. It involves a high-quality oxide insulating layer (such as Al_2O_3 or SiO_2) under the gate, thereby forming a gate structure similar to that of a MOSFET. This allows the GaN HEMT to maintain its high performance while benefiting from the driving simplicity and the enhanced safety features of a MOSFET.

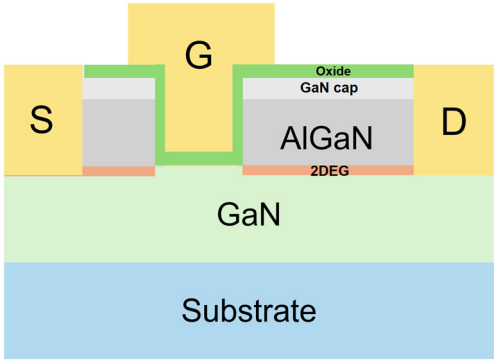


Figure 12. Schematic cross-section of the GaN MOS-HEMT.

3. The Thermal Degradation on GaN HEMTs

3.1. The Threshold Voltage Shift at High Temperatures

The threshold voltage is essential to the performance of the GaN integrated circuits, as its value can influence the on/off state of the device, potentially leading to false triggering. The GaN HEMTs with fluorine implantation are unsuitable for high-temperature applications due to the instability of fluorine concentration over prolonged exposure to high temperatures [48]. The results shown in Figure 13 manifest that the V_{th} of normally-on GaN HEMTs slightly decreases with elevated temperatures, which is around −1 mV/°C [49].

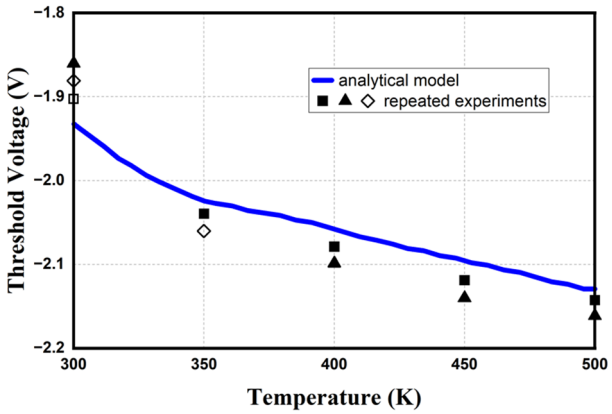


Figure 13. The threshold voltage of AlGaN/GaN HEMT obtained from experiments and an analytical model at different temperatures (created by the authors based on [49]).

However, the introduction of a gate insulator leads to a significant change in the V_{th} shift, which is ascribed to the surface traps in the AlGaN [50]. The mechanisms of threshold voltage shift are different under various temperature conditions. From room temperature to 100 °C, the dominant factor is the traps in the AlGaN barrier, while the threshold voltage shift is more susceptible to the insulator/semiconductor interface traps above 100 °C [51]. To reveal the mechanism of thermally-induced threshold voltage shift in MIS-HEMTs and MOSC-HEMTs, He et al. [52] compared the performance of MIS-HEMTs and MOSC-HEMTs with the same dielectric layer, and the results indicate that the V_{th} shift of MOSC-HEMTs under 200 °C is significantly smaller, as depicted in Figure 14.

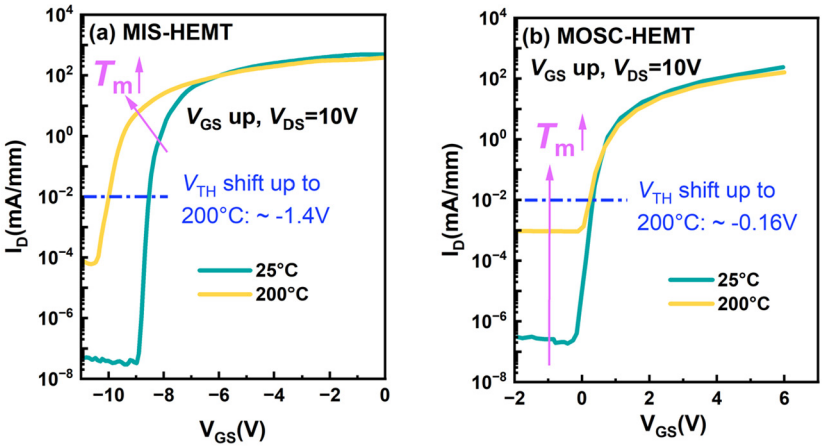


Figure 14. The Vth shift of MIS-HEMTs and MOS-HEMTs (created by the authors based on [52]).

Moreover, the threshold voltage shift can vary depending on the type of insulator used. For instance, a positive shift can be found with high-κ materials, like Gd_2O_2 [53] or ZrO_2 [54], while a negative shift was observed with the moderate-κ material (Al_2O_3) [52]. Moreover, the same material grown by different deposition processes can result in different Vth shifts, such as Al_2O_3 grown by the reactive-ion-sputtered method and atomic layer deposition [55]. The p-GaN gate device also presents a bidirectional voltage shift with different gate types [56]. At elevated temperatures, a positive V_{th} shift was observed in a Schottky-type device, while a negative V_{th} shift was observed in an Ohmic-type device [57].

3.2. The Saturation Current at High Temperatures

The saturation current of GaN-based devices on different substrates, such as SiC and sapphire, significantly decreases with increasing temperature [58,59]. The reduction of output saturation current at high temperatures is caused by phonon scattering [60], resulting in a low carrier mobility [61]. In reference [62], an analytical expression was proposed to calculate the saturation current under different temperature conditions. Husna et al. reported that the introduction of an insulator has a minimal effect on the saturation current in reference [63]. As shown in Figure 15, the saturation current of GaN HEMT and GaN MOS-HEMT decreased by 33% and 32%, respectively, when the test temperature was raised to 200 °C.

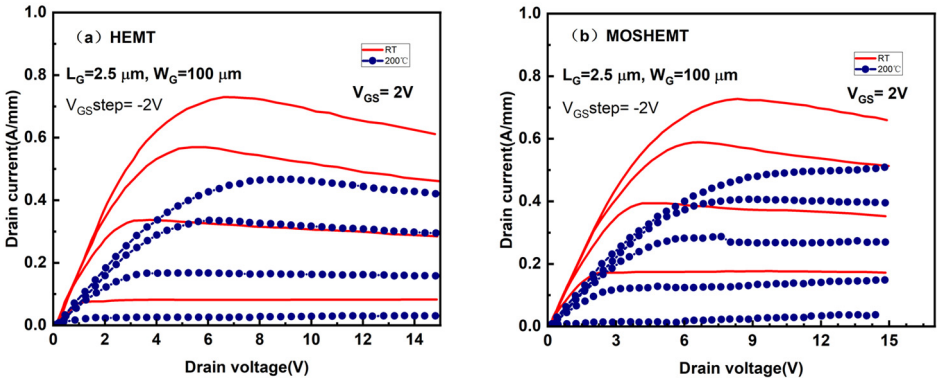


Figure 15. Typical dc output characteristics of AlGaN/GaN (**a**) HEMT and (**b**) MOSHEMT, measured at RT and 200 °C (created by the authors based on [63]).

Moreover, the magnitude of the drain-source current is determined by two factors, carrier sheet density and effective carrier mobility [64]. However, the carrier sheet density remains unchanged at different temperatures in reference [65,66]. Hence, carrier mobility, which is influenced by phonon scattering, is the key factor determining the saturation current. On the other hand, the DC characteristics illustrate that the recessed E-mode GaN HEMT yields a decreased saturation current with elevated temperatures [67]. The transfer curve of p-GaN HEMTs under high temperatures was measured by Keysight 1500 [68]. As illustrated in Figure 16, it can be inferred that the saturation current of p-GaN gate devices decreases due to the elevated test temperature. Concurrently, the on-state resistance experiences an increase, while the trans-conductance undergoes a decrease at elevated temperatures. This phenomenon can be attributed to the reduction in electron mobility. In summary, the saturation current of GaN devices decreases at elevated temperatures, and the gate transconductance is significantly influenced by the electron velocity, which decreases at high temperatures [69]. The transconductance of GaN HEMTs decreases at increased temperatures [70], indicating that the gate control ability degrades under high temperatures.

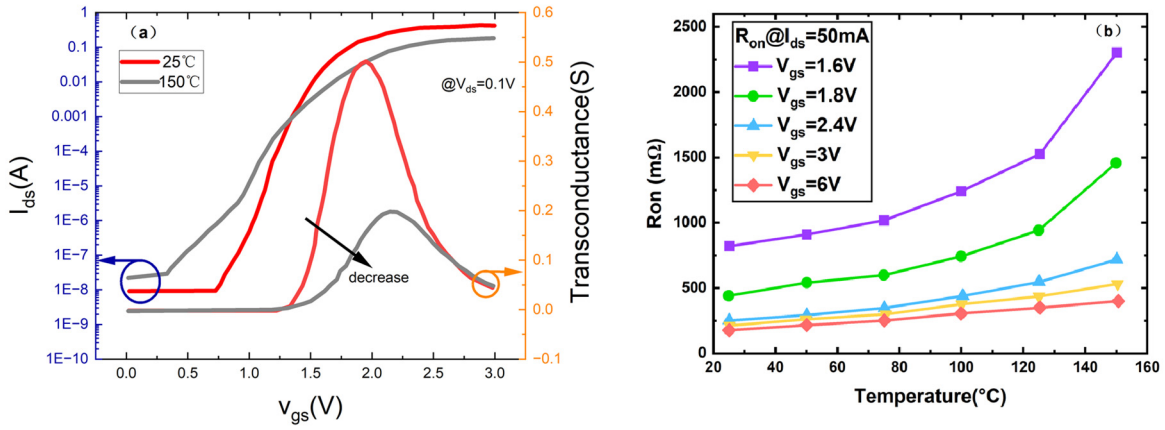


Figure 16. (**a**)Transfer curve of p-GaN HEMT. (**b**) Extracted R_{on} under different V_{gs} from the transfer curve (created by the authors based on [68]).

3.3. The Leakage Currents at High Temperatures

The leakage current was observed to exhibit both negative and positive trends in GaN HEMTs at elevated temperatures. Arulkumaran et al. investigated the mechanism of forward leakage current and found that leakage current decreases with temperatures up to 80 °C [71] in Figure 17, and the negative coefficient of leakage current from 20 °C to 70 °C is due to the impact ionisation [72]. The electrical field of impact ionisation has a positive temperature coefficient, which leads to a reduction in the hole leakage current with increased temperatures [73]. The positive temperature dependence of the gate leakage current is due to the surface hopping conduction mechanism [73] and temperature-assisted tunnelling mechanism [74]. The post-gate annealing was proposed in reference [75] to reduce the gate leakage current by removing shallow traps and activating deeper traps. The reverse-bias leakage current was analysed in reference [76], and the results indicated that the leakage current is dominated by trap-assisted tunnelling transport below 500 K, while thermionic field emission becomes dominant from 500 K to 600 K. The leakage current under high temperatures can be reduced by the introduction of a gate dielectric layer. Figure 18 shows the leakage current of GaN HEMTs and MIS HEMTs at various temperatures [22]. The leakage current of MIS HEMTs is two orders of magnitude smaller than that of HEMTs at 600 °C. Liu et al. [77] studied the mechanism of forward gate leakage current in Al_2O_3/AlGaN/GaN metal-oxide-semiconductor HEMTs (MOS-HEMTs), and the results illustrate that Fowler-Nordheim (F-N) tunnelling is dominant at low temperatures($T < 0$ °C), while trap-assisted tunnelling (TAT) prevails from 0 °C to 200 °C. Xu et al. found that the dominant leakage mechanism in p-GaN devices is the thermionic field emission caused by high-leakage Schottky contacts, whereas Poole-Frenkel emission(PFE) dominates in low-leakage Schottky contacts [78].

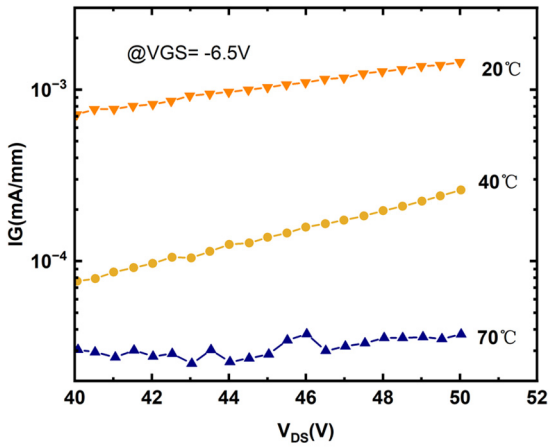


Figure 17. The leakage current under different temperatures of GaN HEMTs (created by the authors based on [71]).

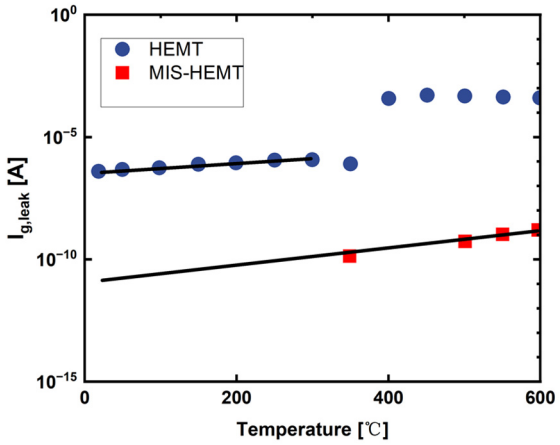


Figure 18. Leakage current of GaN HEMTs and MIS HEMTs under different temperatures (created by the authors based on [22]).

3.4. The Dynamic Resistance at High Temperatures

The degradation of dynamic ON-resistance (dynamic R_{ON}) is a major challenge for GaN HEMTs in power applications, originating from buffer traps, surface states, and threshold voltage (V_{TH}) shift. Tanaka [79] indicated that high temperatures from 100 °C to 200 °C can lead to an increase in the dynamic ON-resistance of GaN HEMTs. Li [80] proposed a novel p-GaN drain (PD) structure, which improved the high-temperature degradation of dynamic R_{ON}. With this structure, the GaN enhancement-mode HEMT (E-HEMT) can achieve enhanced hole compensation at elevated temperatures, resulting in superior dynamic ON-resistance performance. Rathaur [81] demonstrated a quaternary InAlGaN/GaN MIS-HEMT with excellent initial performance and high-temperature stability, exhibiting only a 29% degradation in dynamic ON-resistance at 150 °C.

3.5. The Metallization at High Temperatures

Incorporating titanium nitride (TiN) into the ohmic metal layer of a HEMT has been demonstrated to enhance the thermal stability of the ohmic contact. Zhu et al. [82] proposed ohmic contacts with TiN/Ti/Pt/Au and TiN/Pt/Au. The performance of the TiN/Pt/Au ohmic contact demonstrates minimal sensitivity to variations in annealing temperature. In contrast, the specific contact resistance of the TiN/Ti/Pt/Au ohmic contact exhibits a modest increase with increasing annealing temperature. The good temperature stability of regrown contacts and alloyed contacts was evaluated using TEM and TLM testing by Niroula et al [83]. The results indicated that prolonged exposure to high-temperature environments did not cause significant degradation of crystal structure or metallization properties. This study proposes an ohmic contact technology solution for gallium nitride transistors operating in high-temperature environments. Zhang et al. [84] proposed a Au-free Ti/Al/Ti/TiN ohmic contact annealed at 550 °C, which achieved a smaller contact resistance and specific contact resistivity, while avoiding the AlGaN surface nitrogen vacancy defects and oxidation issues caused by traditional high-temperature annealing. High-temperature environments present a significant challenge

for HEMTs, as they are susceptible to degradation of the gate metals. Rasel et al. [85] observed a significant reduction in gate contact area at 470 °C, along with Ni/Au intermixing near the gate/AlGaN interface. Klein et al. [86] examined the high-temperature thermal stability of three gate metal stacks. The following gate types are distinguished: W-gate, Pd-gate, and Pt/Au-gate. At 600 °C, the Pt/Au-gate stack demonstrated the minimal V_{th} drift and the most substantial I_{on}/I_{off} discrepancy, thereby substantiating its preeminence as the optimal selection for gate metal.

4. Application of GaN Circuits at High Temperatures

Figure 19 shows a summary of high-temperature GaN integrated circuits, and there is an upward trend in the maximum operating temperature of GaN circuits. The maximum operating temperature of complex circuits remains between 200 °C and 350 °C. The GaN circuits can be integrated on different substrate materials, such as Si, SiC, and diamond. The GaN on Si substrate was used in references [87,88], and the operating temperature of GaN circuits can surpass 500 °C. These results indicate an increasing trend of GaN integrated circuits for high-temperature operations.

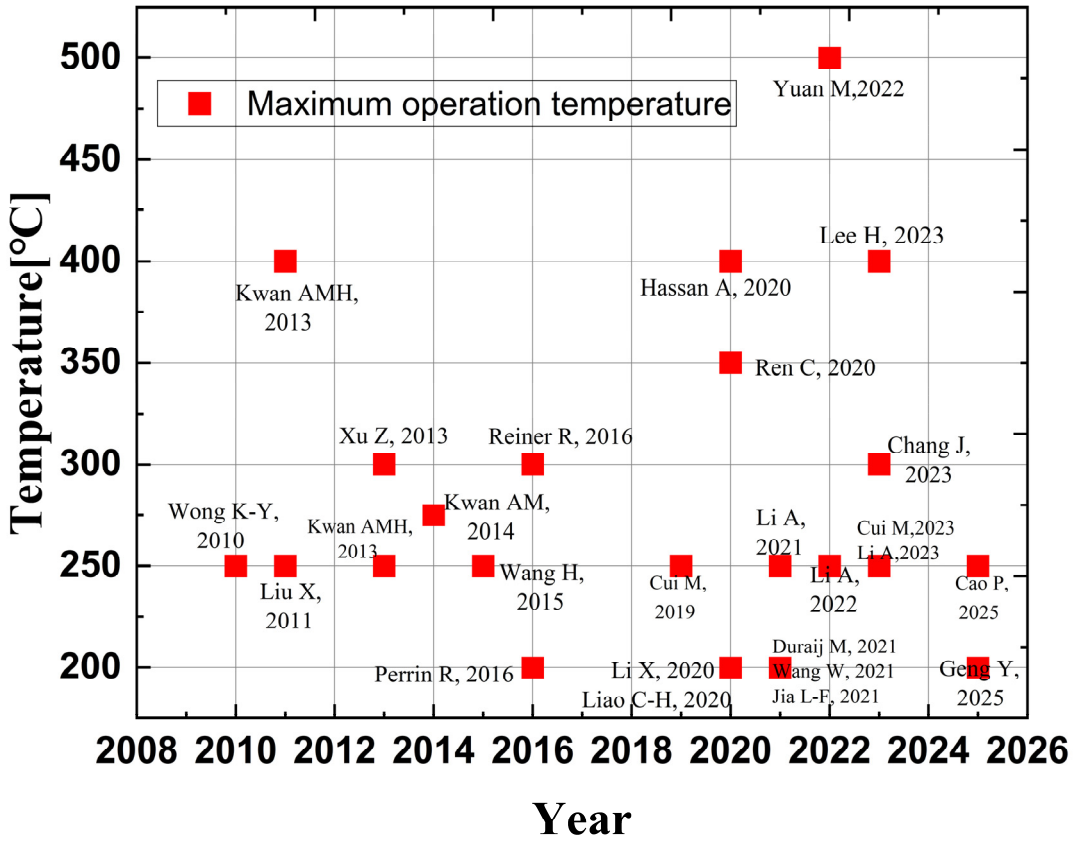


Figure 19. Development of GaN-based circuits for high temperature applications [87–113].

4.1. Power Supply Circuits

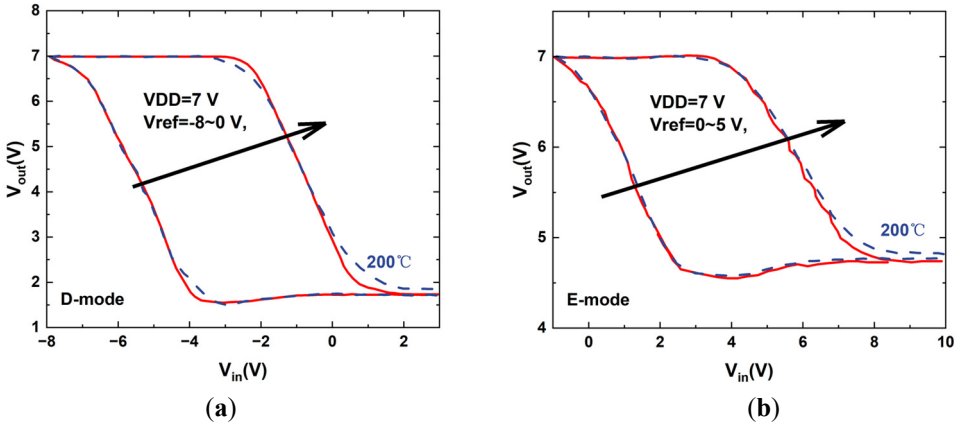
Owing to the high electron mobility and good thermal conductivity of GaN material, power supply circuits based on GaN devices are proper for high temperature and high-frequency applications. A GaN voltage reference generator based on fluorine ion implantation achieves a negative reference voltage (−2 V), and the average drift of the reference voltage is less than 0.5 mV/°C from 25 °C to 250 °C [89]. However, the positive reference voltage is more desirable for power electronics to ensure safety operation. Hence, a reference generator based on MIS-HEMT technology was proposed with a positive supply voltage (2.53 V), and the temperature coefficient of this work is 26.2 ppm/°C [90]. The proportional to absolute temperature (PTAT) voltage source incorporates F-ion-based GaN devices, demonstrating a maximum operating temperature of 250 °C, and the average temperature drift of this voltage source is 0.35 mV/°C [91]. Moreover, Liao et al. proposed a reference generator based on p-type gate GaN HEMTs with a temperature coefficient of 23.6 ppm/°C from -50 to 200 °C [92]. Cao et al. proposed a reference generator with a temperature coefficient of 22.1 ppm/°C [93].

4.2. Comparators

In integrated circuits, comparators play a crucial role in performing essential functions such as signal comparison and level conversion. Table 1 lists the voltage gain, bandwidth, and voltage comparison range of various GaN comparators at high temperatures. Most of the comparators are amplifiers with differential pairs. When one input of the differential pair is connected to a reference voltage, the other is the sampling signal, thus realizing the functionality of the comparator. The comparator in reference [94] is based on fluorine ion implantation technology, and it demonstrates a gain exceeding 31 dB and a bandwidth surpassing 4 MHz at 250 °C. The performance of the comparator that utilizes the same gate process technology is superior, achieving a higher voltage gain of 32 dB and a bandwidth of 2.47 MHz at 250 °C [95]. Additionally, the voltage comparison range has been expanded to 1–6 V [95]. This comparator was utilized to achieve a sawtooth generator and a pulse width modulation (PWM) [96]. The MIS-HEMT technology can reduce the leakage current and improve the performance of GaN devices. A monolithically integrated GaN comparator based on MIS-HEMTs achieves an extended voltage comparison range (3 to 9 V) from RT to 250 °C [97]. In reference [98], the differential pairs include two E-mode GaN MIS-HEMTs, and the performance of the comparator with D-mode differential pairs was also evaluated. The comparison range is from −8 V to 0 V and 0 V to 5 V for D-mode and E-mode differential pairs, respectively. Both comparators can operate at 200 °C, as indicated in Figure 20. Moreover, a 2-step comparator based on p-GaN gate devices was proposed in reference [99] with a gain of 53 dB at 200 °C. As the temperature increases, the GaN comparators exhibit a decreasing trend in the voltage gain, which is attributed to the reduction in effective conductance of GaN devices. Based on GaN comparators, several complex integrated circuits were proposed. A GaN sawtooth generator in Figure 21a can produce a high-amplitude sawtooth signal at 500 kHz with a magnitude of 6.1 V at 250 °C [97]. Moreover, the GaN sawtooth generator in Figure 21b can be applied to generate a PWM circuit. This work is capable of generating a 1 MHz signal at 250 °C, and the duty cycle of the signal is efficiently modulated by the reference voltages with excellent linearity [96].

Table 1. A list of GaN comparators at high temperatures.

Reference	Year	Technology	Temperature	Voltage Gain	Bandwidth	Comparison Range
[94]	2011	F-implantation	250 °C	>31 dB	>4 MHz	0.5–2 V
[95]	2011	F-implantation	250 °C	32.0 dB	2.47 MHz	1–6 V
[96]	2015	F-implantation	250 °C	-	-	0.6–2 V
[97]	2021	MIS-HEMT	250 °C	-	-	3–9 V
[98]	2021	MIS-HEMT	200 °C	-	-	0–5 V
[99]	2025	p-type gate	200 °C	53 dB	-	4–7 V



(**a**) (**b**)

Figure 20. DC output characteristics of GaN comparators by (**a**) D-mode (**b**) E-mode differential pairs at 200 °C, respectively (created by the authors based on [98]).

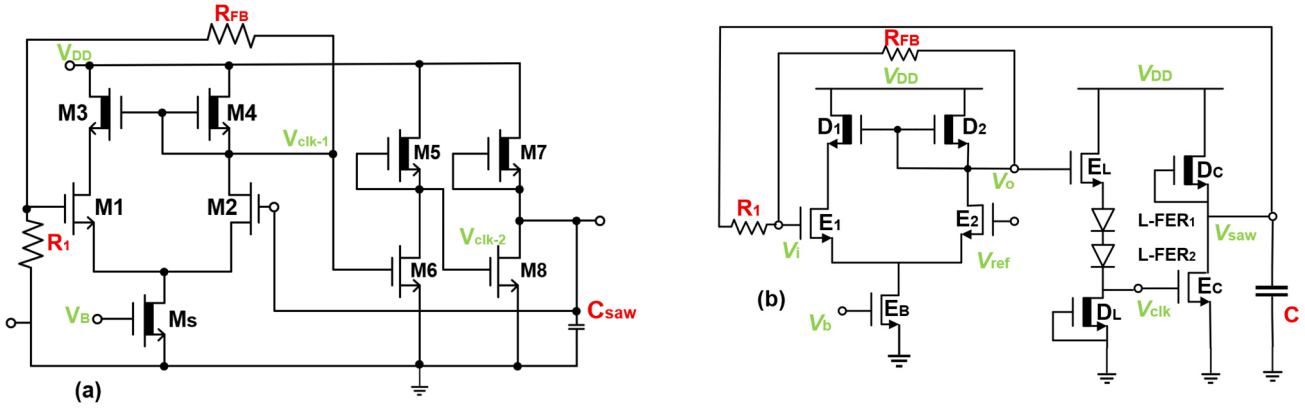


Figure 21. Circuit schematic diagram of the sawtooth waveform generator, (**a**) [97] and (**b**) (created by the authors based on [96]).

4.3. Inverters

A GaN inverter was proposed in reference [12], serving as a fundamental logic block in digital circuits. It consists of a D-mode GaN HEMT and an E-mode GaN HEMT to construct a direct coupled FET logic (DCFL), as illustrated in Figure 22. Table 2 compares the operating temperatures and logic high/low noise margins of different GaN inverters.

Table 2. A list of GaN inverters at high temperatures.

Reference	Year	Technology	Temperature	NML/NMH
[12]	2007	F-implantation	375 °C	0.1/0.3 V
[100]	2014	Recessed gate	300 °C	2.4/3.4 V
[101]	2020	Diamond PMOS	350 °C	-
[102]	2021	p-type gate	200 °C	0.68/1.72 V
[103]	2020	GaN 500	500 °C	2.2/- V
[87]	2023	Recessed gate	400 °C	-

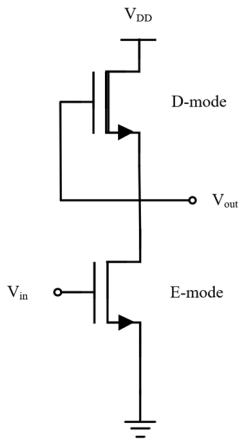


Figure 22. GaN inverter circuit schematic diagram.

Although the temperature increases to 375 °C, the GaN inverter in reference [12] consistently operates with a logic low noise margin (NML) of 0.1 V and a logic high noise margin (NMH) of 0.3 V, as shown in Figure 23. The fluorine ion implantation GaN inverter degrades at high temperatures due to the poor thermal stability of F- ion in the AlGaN layer.

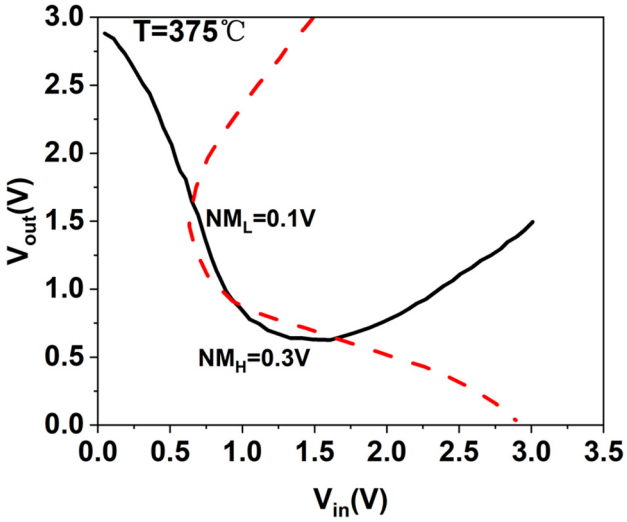


Figure 23. The transfer characteristics of fluorine ion implantation GaN inverters at 375℃ (created by the authors based on [12]).

To improve the high temperature performance, the inverter incorporates a gate-recessed E-mode GaN HEMT, which improves NML and NMH to 2.4 V and 3.4 V with a voltage swing of 6.5 V, respectively [100]. Figure 24 shows that a V_{OH} of 7 V and a V_{OL} of 0.5 V are achieved at 300 ℃, indicating good performance at high temperatures.

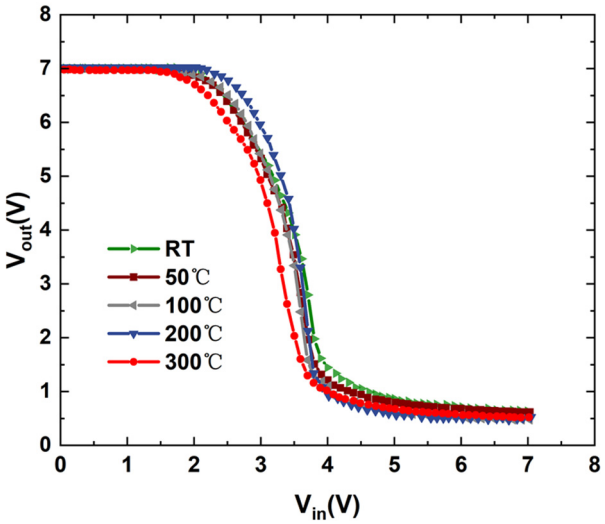


Figure 24. The transfer characteristics of recessed gate GaN inverters at 300℃ (created by the authors based on [100]).

The DCFL inverter based on MIS-HEMTs can reduce the off-state leakage current at high temperatures, which increases its operation temperature to 400 ℃ [87]. In reference [101], the p-type GaN device was fabricated on the diamond substrate. The inverter consists of an n-type D-mode MIS-HEMT and a p-type diamond GaN device, and it exhibits robust functionality even under a high temperature of 350 ℃. As depicted in Figure 25, from 25 °C to 350 °C, the MIS-HEMT inverter experienced a V_{th} drift of approximately 2.4V. The p-GaN gate technology was also applied in the inverter circuit, with a maximum operation temperature of 200 ℃ [102]. The high temperature performance of the p-type GaN inverter degrades as the threshold voltage of the p-type device decreases in Figure 26. The maximum temperature of the GaN inverter, as reported in reference [103], is based on GaN 500 technology, which has a maximum operation temperature of 500 ℃.

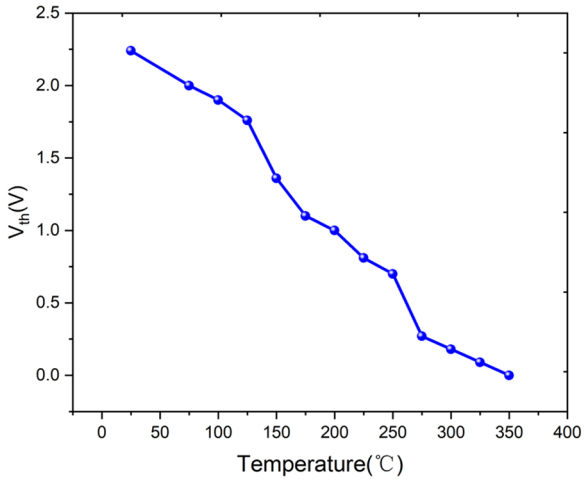


Figure 25. The V_{th} drift of recessed gate GaN inverters at 25–350 °C (created by the authors based on [101]).

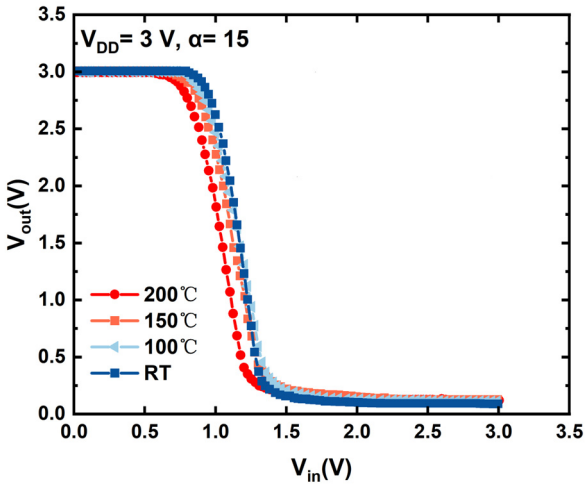


Figure 26. The transfer characteristics of p-type gate GaN inverters at 200 °C (created by the authors based on [102]).

The load-Shift Ketyig (LSK) demodulator, based on the inverter proposed in reference [103], remains fully operational at elevated temperatures up to 400 °C. It can detect a minimum amplitude difference of 1 V between the high voltage level (HVL = ±5 V) and the low voltage level (LVL = ±4 V) of the modulated signal, with a total power of 3.4 W. Based on the DCFL inverter [12], a 17 stage ring oscillator was proposed. The operation temperature of the oscillator is 375 °C.

4.4. Temperature Sensors

Compared to traditional Si MOSFETs, GaN devices are preferred for high-temperature sensors owing to their high temperature tolerance, excellent electron mobility, and compatibility with high-power applications. The temperature sensors based on F-ion implantation technology were proposed in [104] with a temperature sensitivity of −6.9 mV/°C. However, the temperature sensor based on the same gate process can achieve a temperature sensitivity of 0.35 mV/°C with a smaller area (0.207 mm^2) [91]. Both sensors operate within a temperature range of 25 °C to 250 °C. These two temperature sensors present the change of temperature at different voltage levels. Another method to reflect temperature variation involves using resistors with a sensitivity of 10 Ω/°C from 25 °C to 175 °C [105]. Moreover, the temperature sensor based on a GaN Schottky barrier diode can work from 25 °C to 200 °C [106]. The GaN MIS-HEMT temperature sensor with a sensitivity of 15.86 mV/°C was proposed in reference [107] with a circuit area of 0.05 mm^2. The temperature sensor based on a p-GaN/AlGaN/GaN heterostructure with a sensitivity of 19.7 mV/°C was proposed in reference [108]. The detailed comparison of GaN temperature sensors is listed in Table 3.

Table 3. Performance summary of GaN temperature sensors.

Reference	Year	Technology	Temperature Range (℃)	Temperature Sensitivity (mV/℃)	Area (mm^2)
[104]	2013	F-implantation	25–275 ℃	−6.9	1.23
[91]	2014	F-implantation	25–250 ℃	0.35	0.207
[105]	2016	GaN HEMT	25–175 ℃	10	-
[106]	2020	GaN SBD	25–200 ℃	1.6	0.2
[107]	2023	MIS-HEMT	25–250 ℃	15.86	0.05
[108]	2023	P-GaN/AlGaN/GaN	25–300 ℃	19.7	-

4.5. GaN DC-DC Converters

To fully realise the advantages of GaN devices at high temperatures, monolithic GaN DC-DC converters for high-temperature applications were proposed [109,110]. In Reference [109], a gate driver for GaN DC-DC converters was designed as shown in Figure 27. The GaN gate driver circuit includes DFCL inverters and a buffer stage, and the converter shows only 11% reduction of the output voltage at 250 ℃. Based on this driver design, Cui et al. proposed a synchronous buck converter with good thermal stability from 25 ℃ to 250 ℃, as shown in Figure 28 [110]. At high temperatures, the turn-on and turn-off processes of the GaN device become slow due to the reduction of charging and discharging currents. Consequently, the high-side and low-side power transistors may be simultaneously conducted. To ensure safe operation of DC-DC converters at high temperatures, a monolithically integrated GaN deadtime generator was proposed for GaN DC-DC buck converters in reference [111]. The results indicate that a deadtime of less than 0.13 μs is achieved at 250 ℃, and the peak efficiency of the proposed converter is 80% at high temperatures. In Reference [112], an active clamp flyback inverter achieved a switching frequency of 800 kHz at 200 °C. Martijn et al. verified the hypothesis that switching capacitance increases at high temperatures and affects power losses in a half-bridge switching stage [113]. These results validate the advantages of GaN devices and integrated circuits for high-temperature power converters in applications under extreme environments.

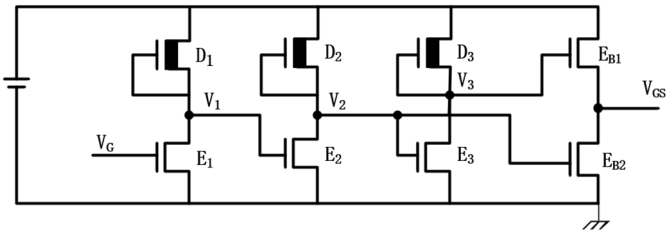


Figure 27. The circuit diagram of the GaN gate driver (created by the authors based on [109]).

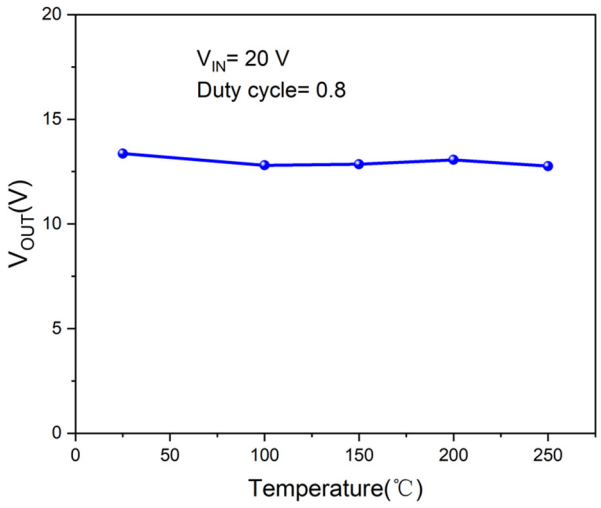


Figure 28. Experiments results of synchronous converter at various tempetatures and duty cycles (created by the authors based on [110]).

5. Conclusions

GaN demonstrates significant potential as a material for power electronics, particularly in high-temperature semiconductor applications. This review summarises GaN device properties and applications at various temperatures, including saturation current, leakage current, on-state resistance, transconductance, and threshold voltage. Solutions are summarised to reduce the temperature drift of specific parameters. The review also offers a comprehensive discussion on thermal degradation mechanisms of their properties. Furthermore, the performance of GaN integrated circuits at various temperatures is reviewed to investigate their potential for temperature applications. Despite the acceptable performance degradation at high temperatures, the thermal reliability of GaN devices, along with their ability to operate at higher frequencies, positions them as a promising candidate for high frequency and high efficiency power electronics under extreme environments.

Author Contributions

K.Z.: Validation, Visualization, Writing—Original Draft, and Writing—Review & Editing; P.C.: Validation, Visualization, Writing—Original Draft, and Writing—Review & Editing; J.J.: Validation, and Writing—Review & Editing; Y.X.: Review & Editing; Z.L.: Review & Editing; F.X: Review & Editing; M.C.: Supervision, Project Administration, and Writing—Review & Editing.

Ethics Statement

Not applicable.

Informed Consent Statement

Not applicable.

Data Availability Statement

All data included in this study are available upon request by contact with the corresponding author.

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Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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