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# Decoupled Design of Inverter Output Impedance for Parallel Operated Inverters: An Analytical Approach

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**ABSTRACT:** This paper suggests an analytical framework to design the output impedance of a microsource inverter to meet the requirements of proportional load sharing with the permissible range of THD (total harmonic distortion) of the output voltage as per the IEEE 519 standard. In order to achieve the aforementioned objectives, the integral controller is designed in such a way as to make the output impedance of an inverter capacitive in nature. The optimum design of capacitive output impedance at the harmonic frequencies ensures reduced THD levels in the output voltage without affecting proportional load sharing, which is determined by fundamental frequency impedance, ensuring the decoupled design to meet different requirements at the same time. The focus of the work is also laid on the inherent limitations of conventional droop control of inverters and its remedial measures through bolting a regulator on its control loop. The modification of the robust droop control structure for a capacitive inverter is discussed, and small signal stability/PF (participation factor) based analysis is done to ensure the steady state stable operation. In order to enhance the load voltage quality further, a bypassing the harmonic current components strategy is discussed and developed further, which led to $THD_v < 5\%$. Subsequently, the basic stability analysis is conducted to determine the finite parameters of BHC by control system principles. The discussed models and schemes are simulated under both linear and nonlinear load conditions to validate the proposed strategies, and their effectiveness is assessed through a comparative analysis.

**Keywords:** Power sharing; Power quality; Stability; Total harmonic distortion

## 1. Introduction

The concept of microgrid emerged in the early 2000 and initially it was proposed as a means/solution of integrating renewable energy resources. These energy resources are not available round the clock due to their volatile and intermittent nature. Therefore, it was not easy to connect them in large quantities, and consequently, the idea of a microgrid was laid down. However, the renewable energy resources have received a lot of attention in recent years because of their self-renewal nature over the passage of time,

deterioration, and depletion of the global environment and energy. The integration of renewable energy based distributed energy resources is demanded by the power system community to achieve the objectives of reliable, economical, and carbon-free supply [1,2]. Most of these resources are interfaced with the utility grid by power electronic based converters. Due to the negligible inertia of power converters, the stability issues in such systems remain a matter of concern. However, maintaining the system stability in the face of fluctuating microgrid operating conditions is also a crucial design problem. The study, which examines the stability issues using a single-phase community microgrid concept, was conducted in [3]. On the other hand, the presence of rotating inertia in the conventional synchronous alternators assists in stabilizing the system via the well-known droop control concept, which originates from the principle of power balance in synchronous machines. An imbalance between the input mechanical power and the output electric power causes a change in the rotor speed and electrical frequency. Similarly, the variation in output reactive power results in voltage magnitude deviation. Such characteristics can be artificially created for an electronically interfaced inverter-based AC microgrid [4].

The mechanisms of active and reactive power regulation through droop control, and their effects on voltage and frequency, have been studied in the past. The form of the droop equations varies depending on the nature of the inverter's output impedance, which may be resistive, inductive, or capacitive.The output Impedance of the power inverter plays an important/crucial role in improving the quality of the output voltage. Inverter designed with resistive and inductive output impedances have different levels of total harmonic distortion in the output voltage [4,5]. Besides this, inverter output impedance also controls the load sharing accuracy of various VSI units connected in parallel [6]. The parallel operation of inverters becomes important when it comes to the availability of high current power electronic devices, system redundancy, reliability expected by critical customers, *etc.* The issues of thermal management and design of high power inverters are expected to be alleviated by parallel operation. Therefore, the challenge of sharing the load among parallel operated inverters is required to be addressed well [7].

However, the power converters, which are equipped with the conventional droop controllers to share active as well as reactive power, have inherent limitations of inaccurate sharing of power, circulating current, *etc.* One such issue in the low voltage dc microgrid is addressed, and its solution is proposed by adaptive droop control that minimizes the difference between circulating currents via a virtual resistor [8]. The presence of a nonlinear load in the conventional control is also a problematic situation as far as the quality of load voltage and grid current waveform is concerned [9]. The intrinsic drawbacks of the typical droop controller include erroneous power sharing to the load as a result of mismatched output impedances between inverters, noise, disturbances, numerical computations, mismatched components, *etc.* An uncertainty and disturbance estimator based droop control is proposed to address these issues [10]. Various solutions are reported in the literature to address the aforesaid issues in the past. In this order, Ref. [11] presents the limitations of the CDC (conventional droop control) and then modifies the droop control structure in a robust form, thereby avoiding the condition of the same per unit output impedance between parallel inverters. Inverters are classified as inductive, resistive, or capacitive according to the nature of their output impedance, and each type is associated with a corresponding droop control equation[12]. A universal droop control strategy, which adopts the droop control formulation of a resistive inverter, is proposed in [13] for inverters with an output impedance angle ranging from $-\pi/2$ to $+\pi/2$ radians.The same model of resistive inverter is shown to be stable in the output impedance angle range of $-\pi/2$ to $+\pi/2$ radians through a small signal stability tool [14]. The parallel operation of inverters with different types of output impedance is made possible by universal droop controllers; however, droop controllers still have to trade-off between power sharing and load voltage and frequency regulation. This trade-off can be somewhat eliminated by the approach suggested in [15].

The various intrinsic features of microgrid are covered in primary, secondary, and tertiary layers of control. The key features of a multilayer control system are regulating reactive and active power flow to

maintain stable voltage amplitude and frequency, and adding reactive power compensation, harmonic current sharing, and filtering to ensure disturbance rejection and meet power quality standards in microgrids. A network forming three phase isolated inverter model with its primary controls (droop control) is simulated to illustrate its working [16]. In the hierarchical control of a microgrid, the function of restoring voltage and frequency by the secondary layer of control for two network forming converters is illustrated through a case study [17]. A new data-driven distributed control structure is presented employing a droop-free paradigm for voltage/frequency regulation and reactive/active power sharing of islanded microgrids in order to minimize the inherent temporal gap between primary and secondary control [18]. The concept of replacement of primary and secondary droop control by regulators is proposed in [19]. In the literature discussed above [7,10–14], shaping of the output impedance remains at the center to reduce $THD_v$, which requires tuning procedures. To eliminate the need for tuning, the concept of smart impedance, which can perform manipulations, is proposed in [20] to perform the tuning procedure electronically.

However, in light of the literature, discussed above, the simplistic didactic approach to understand proportional power sharing to the load and maintaining the power quality simultaneously is still missing. Therefore, keeping this in mind, efforts have been put to achieve the following objectives in a comprehensive manner.

(1) To discuss robust droop control for proportional power sharing and design the integrator coefficient of the inverter output impedance to ensure reduced THD in the output voltage.
(2) To discuss and modify bypassing the current component strategy for enhanced output voltage.

The paper is organized as follows. Section 2 discusses the deterioration mechanism of voltage with its mathematical foundation. Section 3 presents the design of the integrator coefficient for the capacitive inverter, followed by the modified BHC strategy in Section 4 to further improve the output voltage quality. The small signal model of capacitive type inverter is obtained in Section 5 followed by basic stability analysis for the BHC equipped inverter. Section 6 discusses the inherent limitations of CDC and presents a robust droop control (RDC) scheme as a remedial measure to address these limitations. Various scenarios and detailed simulations are discussed in Section 7. Section 8 concludes the paper.

## 2. Deterioration of Voltage: An Underlying Mechanism

Various renewable energy sources, such as tidal, wind, and solar power, are increasingly being developed. Microgrids are commonly formed using power inverters, which may or may not be connected to the grid. Degradation in the voltage supplied by inverters is a significant power quality issue in these applications [7]. This section focuses on the underlying mechanism behind the degradation of voltage quality.

The output voltage of such an inverter, modeled in Figure 1a, is expressed in Equation (1) by referring its equivalent circuit in Figure 1b.

$$V_o = v_r - Z_o(s)\, i \tag{1}$$

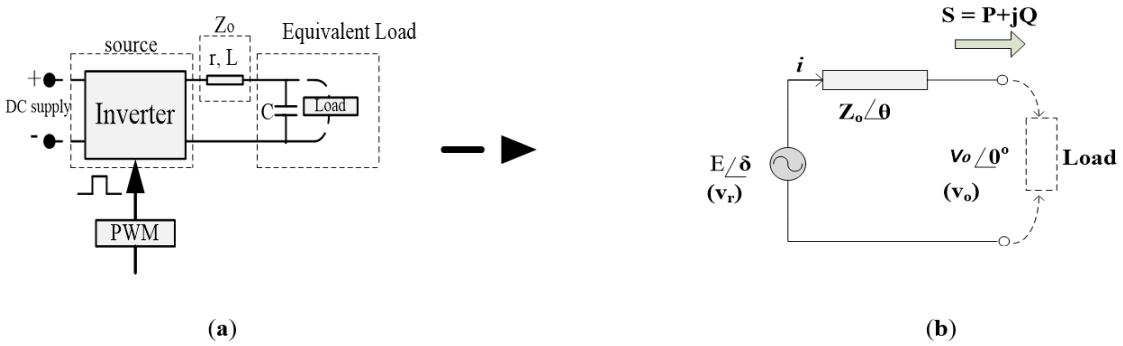



**Figure 1.** (**a**) Inverter model; (**b**) Equivalent circuit.

Where E (volt) and δ (radians) are the magnitude and phase angle of the reference voltage $v_r$; $Z_o$ (Ω) and θ (radians) are the magnitude and angle of inverter output impedance; S, P and Q are apparent, active and reactive power; $V_o$ (volt) is the voltage across the output terminals, and *i* (amp) is the current flowing through $Z_o$.

The current *i* contains harmonics due to the inclusion of nonlinear load or/and the PWM in the inverter, thus causing harmonic voltage drop in the impedance, $Z_o$. Harmonic voltage components appearing in the output voltage will degrade the output voltage and induces total harmonic distortion (THD) provided the reference voltage is free of harmonics. THD may also appear in the output voltage due to harmonic components in the voltage reference, $v_r$. One possible solution to make the output voltage harmonic free, is to keep the reference voltage clean. Additionally, the magnitude of the inverter output impedance should be as small as possible over the range of dominant harmonic frequency components. Another way is to deroute harmonic current components from current *i*, in order to make it clean. In the third option, the reference voltage ($v_r$) should provide an adequate amount of harmonic voltages ($v_{oh}$) to neutralize the harmonic voltage drops in the output impedance, $Z_o$.

### *2.1. Impact of Inverter Output Impedance*

In this section, the mathematical relationship between the inverter output impedance and $THD_v$ is established. The inverter current *i*, as shown in Figure 1, can be expressed in terms of its harmonic components as follows.

$$i = \sqrt{2}\sum_{h=1}^{\infty} I_h \sin(h\omega t + \Phi_h) \tag{2}$$

where *h* is the harmonic order number. The $\omega$ and $\Phi_h$ are angular frequency (radians/sec) and *h*-th phase angle (radians) respectively.

The fundamental component of $v_o$ is expressed as

$$v_{o1} = v_r - \sqrt{2}\, I_1 |Z_o(j\omega)| \sin(\omega t + \Phi_1 + \theta) \tag{3}$$

assuming that the voltage reference $v_r$ is clean and sinusoidal, which is expressed in Equation (4).
where

$$v_r = \sqrt{2}\, E \sin(\omega t + \delta) \tag{4}$$

$$v_{o1} = \sqrt{2}\, V_1 \sin(\omega t + \beta_o) \tag{5}$$

where

$$V_1 = \sqrt{(E^2 + I_1^2 |Z_o(j\omega)|^2 - 2\, E\, I_1 |Z_o(j\omega)| \cos(\Phi_1 + \theta - \delta))} \tag{6}$$

and

$$\beta_o = \tan^{-1}\left(\frac{I_1 |Z_o(j\omega)| \sin(\Phi_1 + \theta - \delta)}{I_1 |Z_o(j\omega)| \cos(\Phi_1 + \theta - \delta) - E}\right) \tag{7}$$

Now the output voltage harmonic components would be

$$v_{oh} = \sqrt{2}\sum_{h=2}^{\infty} I_h |Z_o(jh\omega)| \sin(h\omega t + \Phi_h + \angle Z_o(jh\omega)) \tag{8}$$

By referring Equation (8), it is clear that $v_{oh}$ depends upon harmonic current components and impedance at harmonic frequencies. The fundamental component of output voltage, $v_{o1}$ is determined by reference voltage, fundamental current and output impedance at fundamental frequency. It is evident from this analysis that $v_{oh}$ is not affected by $v_{o1}$ and this feature can be used to design the impedance for different purposes. The output impedance at harmonic frequencies can be reduced for a selected value of virtual capacitance, connected in series with filter inductor, in order to reduce per unit THD of the output voltage, expressed in Equation (9). On the other hand, objective of proportional load sharing is governed by the

design of fundamental output impedance. Therefore, the optimum design of a virtual capacitor at high harmonic frequencies decouples to meet the requirements of proportional load sharing and low $THD_v$ [7].

$$THD_v = \frac{\left(\sum_{h=2}^{\infty} |Z_o(jh\omega)|^2 I_h^2\right)^{\frac{1}{2}}}{V_1} \quad (9)$$

In order to further analyse the source of harmonics in the output voltage and its mitigation measures, the circuit model of Figure 1b is redrawn in Figure 2 for a particular *h*-th harmonic component. The following set of equations are written by referring Figure 2a.

$$v_r = v_{r1} + v_{r2} + v_{r3} + \ldots + v_{rh} \quad (10)$$

$$i = i_1 + i_2 + i_3 + \ldots + i_h \quad (11)$$

and,

$$v_o = v_{o1} + v_{o2} + v_{o3} + \ldots + v_{oh} \quad (12)$$

The superposition theorem allows us to decompose this circuit into multiple *h*-th order circuits for analysis purposes. The circuit shown in Figure 2b is the *h*-th order decomposed circuit. If $v_{oh} = 0$, then only the current source is left in the right part of the circuit, shown in Figure 2b. Ideally, the function of an inverter should be to supply power at the right voltage and frequency as per standards/laws. If multiple inverters are working in conjunction, the proportional sharing of power is also required at the fundamental frequency. The harmonics in the output voltage should ideally be zero, *i.e.*, $v_{oh} = 0$. ($h = 2, 3, \ldots$) even if the presence of $i_h$ exists. This can be accomplished only when the drop of *h*-th order current on the output impedance is equal to *h*-th order component of the reference voltage.

$$i_h Z_o(j\omega h) = v_{rh} \quad (13)$$

The application of this concept can facilitate the design of a controller to reduce $THD_v$.

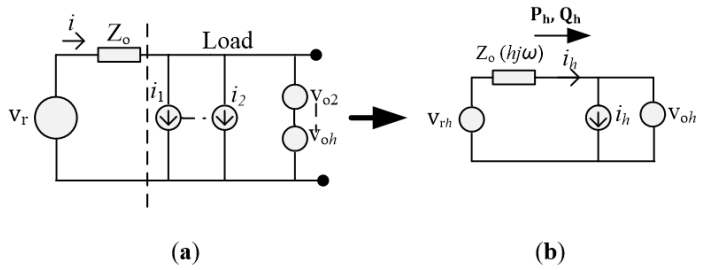



**Figure 2.** (**a**) Inverter circuit showing harmonic components; (**b**) decomposed *h*-th harmonic circuit

## 3. Design of a Capacitive Type Inverter

The objective of designing the capacitive type inverter is to reduce the magnitude of output impedance at dominating harmonic frequency components ($h = 3, 5, ...$), thereby reducing the THD of load or output voltage, in the case of a nonlinear load. The single phase H-bridge insulated gate bipolar transistor (IGBT) inverter circuit with its control circuitry, as shown in Figure 3, is under consideration for designing the capacitive output impedance. The inverter is connected to an AC bus through a switch, where the load is assumed to be connected. The current *i* (current in the filter inductor) can be passed through an integrator block to make the output impedance capacitive, as shown in the closed-loop system in Figure 4 [12].

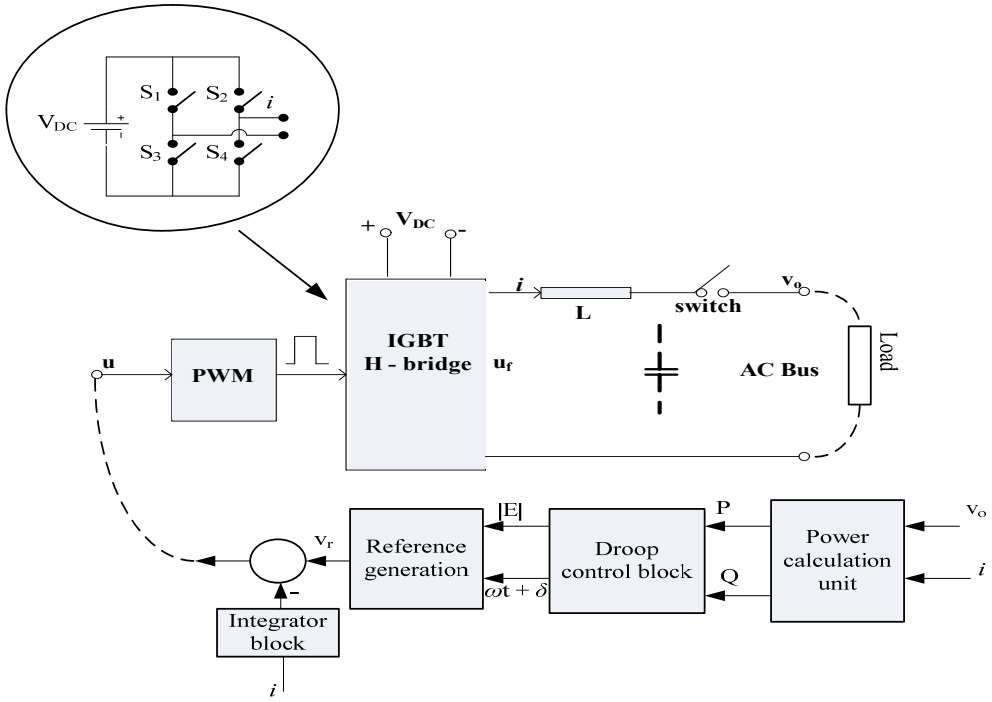



**Figure 3.** Physical implementation of single phase inverter with its control loop.

By referring Figures 3 and 4, the following relationships are expressed in Equation (14).

$$\begin{aligned} u_f &= (r + sL)\, i + v_o \\ u &= v_r - \frac{1}{sC_o}\, i \end{aligned} \tag{14}$$

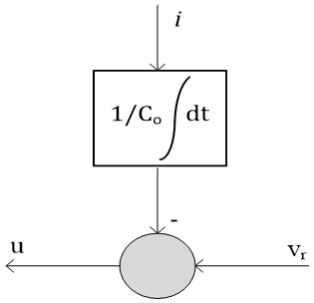



**Figure 4.** Controller for achieving capacitive output impedance.

Since the average of $u_f$ over a switching period can be approximated by u [7]. Therefore, equating both terms in Equation (14) yields

$$v_o = v_r - (r + sL + \frac{1}{sC_o})\, i \tag{15}$$

where,

Now, output impedance, denoted by $Z_o(s)$, is expressed as follows

$$Z_o(s) = r + sL + \frac{1}{sC_o}$$

Neglecting the parasitic resistance, r (usually small)

$$Z_o(s) \approx \frac{1}{sC_o} \text{ (if capacitor } C_o \text{ is chosen small enough)} \quad (16)$$

At the fundamental frequency, the output impedance can be made almost entirely capacitive if the capacitance $C_o$ is small enough to negate the effect of an inductor. Due to the presence of an integrator block, any dc offset in the current *i*, e.g., that caused by the conversion process or faults in the system, would lead to a dc component in the reference signal and hence in the load voltage. In order to avoid this problem, two solutions are presented.

1. For example, the integrator $\frac{1}{sC_o}$ can be reset when the inductor current passes zero if the offset exceeds a given level.
2. In an alternate solution, the integrator $\frac{1}{sC_o}$ can be slightly modified as $\frac{1}{sC_o + \varepsilon}$ with a negligible positive number $\varepsilon \approx 0$. This is equivalent to putting a large resistor $\frac{1}{\varepsilon}$ in parallel with $C_o$, which does not change the performance at non dc frequencies.

To derive the condition for system stability, we will use the conventional control-system approach. If the controller is implemented digitally, the effect of sampling, PWM conversion, and computation can be approximated by a step delay $e^{-sT_s}$, where $T_s$ is the sampling period. The block diagram of the current loop (Figure 5) is shown below [7].

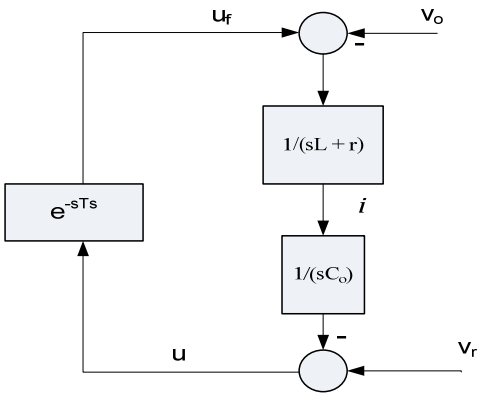



**Figure 5.** Current loop [12].

The corresponding open loop transfer function is given by

$$F(s) = \frac{1}{sC_o}\frac{1}{sL + r}e^{-sT_s} \quad (17)$$

The open loop transfer function has a pole at $s = 0$, and there is no pole in the right half of the *s* plane. Here, the Nyquist plot tool of the control system is used to ensure the stability of the open loop transfer function. According to the condition of stability, in the Nyquist method, the plot should not encircle the critical point (−1, 0) on the real axis of the *s*-plane. If the plot crosses the real axis for the first time at some frequency $\omega_o$, then

$$\frac{-\pi}{2} - \tan^{-1}\frac{\omega_o L}{r} - \omega_o T_s = -\pi \quad (18)$$

Therefore, $\tan(\omega_o T_s) = \frac{r}{\omega_o L}$

The loop gain is given by:

$$\frac{1}{\omega_o C_o \sqrt{r^2 + \omega_o^2 L^2}} \quad (19)$$

The loop gain should be less than 1 at this frequency $\omega_o$, or otherwise, the loop is stable if

$$\frac{1}{C_o} < \omega_o \sqrt{r^2 + \omega_o^2 L^2} \tag{20}$$

where $0 < \omega_o < \frac{\pi}{2T_s}$

Therefore, the loop shown in Figure 4 is stable if

$$\frac{1}{C_o} < \frac{\pi}{2T_s} \sqrt{\left(\frac{\pi L}{2T_s}\right)^2 + r^2} \tag{21}$$

For a small parasitic resistor r, the right hand side of the above equation reduces to $\left(\frac{\pi}{2T_s}\right)^2 L$. The loop will be stable if capacitor $C_o$ or the switching frequency, $f_s = \frac{1}{T_s}$ is chosen large enough so that the sampling frequency $f_s$ is larger than four times of $\frac{1}{2\pi\sqrt{LC_o}}$. Also, in practicality, r is not zero, which assists in maintaining stability.

### *3.1. Analytical Design Process*

As discussed previously in Section 2.1, the THD of the voltage is governed by the inverter output impedance at the harmonic frequencies. In order to make the output impedance capacitive in nature and reduce its magnitude at dominating harmonic frequencies, a virtual capacitance is added in series with the filter inductor. The procedure of obtaining the optimum design of $C_o$ or integrator constant is described below.

The minimization problem can be solved by taking the derivative of the function and then equating it to zero,

$$\frac{d}{dt} f = 0, f \text{ is a function to be minimized} \tag{22}$$

By referring the expression in Equation (9), $THD_v$ can be reduced by minimizing the harmonic voltage drops on the output impedance. Therefore,

$$f = \min_{C_o} \sum_{h=2}^{\infty} i_{1h}^2 \, |Z_o(jh\omega^*)|^2 \tag{23}$$

The magnitude of the output impedance at $h$-th harmonic frequency is expressed in (24) by considering virtual capacitance $C_o$.

where

$$|Z_o(jh\omega^*)| = \left(r + h\omega^* L - \frac{1}{h\omega^* C_o}\right) \tag{24}$$

$h$ and $\omega^*$ are harmonic order and fundamental frequency, respectively. The parasitic resistance, r can be neglected as it has a small value. Minimization of the function $f$ ensures improved THDv for a particular virtual capacitor $C_o$. Differentiating Equation (23) with respect to $C_o$ and equating to zero yields the optimum capacitance, expressed in Equation (25).

$$C_o = \frac{1}{(\omega^*)^2} \frac{1}{L} \frac{\sum_{h=2}^{N} \frac{i_{1h}^2}{h^2}}{\sum_{h=2}^{N} i_{1h}^2} \tag{25}$$

where, $i_{1h} = \frac{I_h}{I_1}$, is $h$-th order normalized harmonic current with respect to fundamental current.

Substituting $C_o$ in Equation (23) yields the following

$$f(C_o) = (L\omega^*)^2 \sum_{h=2}^{N} i_{1h}^2 \left(h - \frac{1}{h} \frac{\sum_{h=2}^{N} i_{1h}^2}{\sum_{h=2}^{N} \frac{i_{1h}^2}{h^2}}\right)^2 \tag{26}$$

It is evident from the above equation that THD is proportional to the inductance L. A small L not only reduces the inductor size and cost, but also it enables a small integrator gain to ensure the stability of the current loop. Assuming odd harmonics ($h$ = 3, 5, 7, …) are equally distributed, Equation (25) will have the form

$$C_o = \frac{1}{(\omega^*)^2}\frac{1}{L}\frac{\sum_{h=3,5,7,\ldots,N}^{N}\frac{1}{h^2}}{\sum_{h=3,5,7,\ldots,N}^{N}1} \quad (27)$$

Assuming the 3rd, 5th, and 7th harmonic components, the optimal capacitance, which is calculated by using Equation (27), is given by

$$C_o = \frac{143}{2500\,(\omega^*)^2 L} \quad (28)$$

The optimal capacitance values, designed for specific harmonic frequencies, are listed in Table 1. The fundamental inverter output impedance ($Z_o$) are too illustrated. The plot of output impedance gain with respect to frequency (Hz) for optimal capacitance (designed for $h$ = 3rd and 5th) is shown in Figure 6b. The output impedance gain at the fundamental frequency is negative and goes from negative to positive at 1142 rad/s.

The suggested method enables the first order design of an integrator for specific harmonic frequency components. Though it is possible to build a topology of an integrator with a higher order, that is not discussed here due to page limitations.

**Table 1.** Optimal capacitance and its corresponding output impedance ($Z_o$).

| Harmonic Number | Optimal Capacitance | $Z_o$ at Fundamental Frequency |
|---|---|---|
| 3rd and 5th | 325 µF | $-j12.23\omega^*L$ (capacitive) |
| 3rd only | 479 µF | $-j8\omega^*L$ (capacitive) |
| 5th only | 172.64 µF | $-j24\omega^*L$ (capacitive) |

### *3.2. Proportional Load Sharing*

Besides low THD in the output voltage, the proportional load sharing between inverters is also recommended. The idea of a robust droop controller arises as the conditions for achieving the aforesaid objectives in the conventional counterpart are not met in practice. In this sub section, the conditions required for proportional load sharing using conventional droop controllers are first derived, followed by a discussion of the robust droop control scheme. The circuit models of two inverters, shown in Figure 6a, with capacitive output impedances, are connected in parallel. The feeder impedance is neglected, and the inverter output impedance dominates between the inverter and the AC bus [11,14].

By referring Figure 1b, the expression of apparent power can be written as

$$S = v_o I \quad (29)$$

$$S = v_o\left(\frac{v_r - v_o}{Z_o \angle \theta}\right) \quad (30)$$

where $v_o$ and $I$ are the RMS values of output voltage and current, respectively. The active and reactive power outputs are expressed as

$$P = \left(\frac{EV_o}{Z_o}\cos(\delta) - \frac{V_o^2}{Z_o}\right)\cos(\theta) + \frac{EV_o}{Z_o}\sin(\delta)\sin(\theta) \quad (31)$$

$$Q = \left(\frac{EV_o}{Z_o}\cos(\delta) - \frac{V_o^2}{Z_o}\right)\sin(\theta) - \frac{EV_o}{Z_o}\sin(\delta)\cos(\theta)$$

For the capacitive output impedance of the inverter, $\theta = -90°$. With this substitution, the active and reactive power of $i$-th inverter are expressed in Equations (32) and (33).

$$P_i = -\frac{E_i V_o}{Z_o} \sin(\delta) \tag{32}$$

$$Q_i = -\frac{E_i V_o}{Z_o} \cos(\delta) + \frac{V_o^2}{Z_o} \tag{33}$$

For a very small angle δ, $P_i \sim -\delta$ & $Q_i \sim -E$; *i* being the number of inverters participating in the parallel operation.

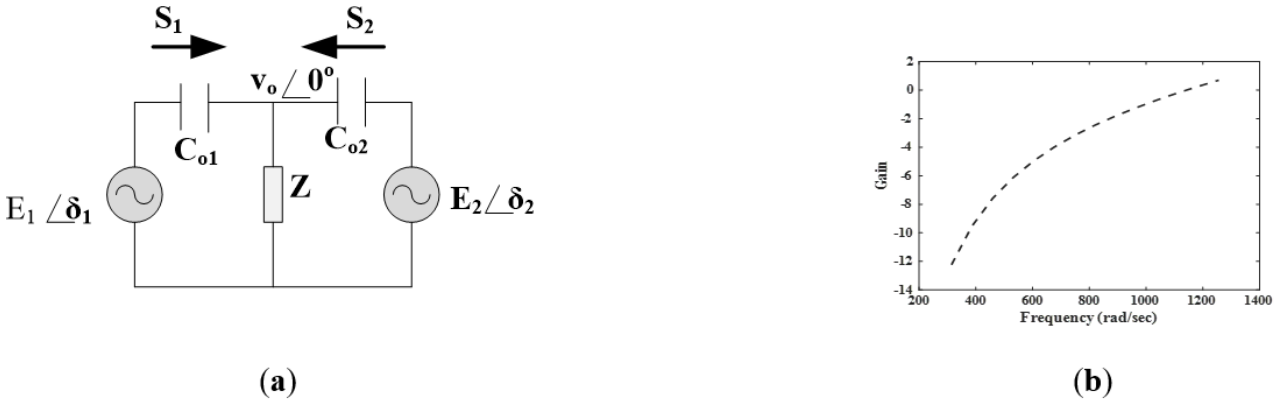



**Figure 6.** (**a**) Two capacitive inverters operated in parallel; (**b**) Gain of output impedance *vs*. frequency.

Therefore, the conventional droop control characteristics for capacitive inverters are shown in Equation (34). The corresponding characteristics are shown in Figure 7.

$$E_i = E^* + n_{iC}\, Q_i \tag{34}$$

$$\omega_i = \omega^* + m_{iC}\, P_i$$

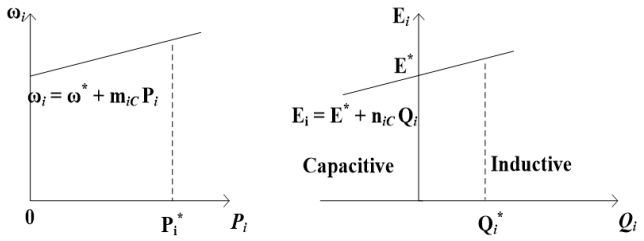



**Figure 7.** Droop control characteristics for capacitive inverter

### 3.2.1. Reactive Power Sharing

Substituting Equation (34) into (33), the expression of the reactive power of *i*-th inverter is written as follows

$$Q_i = \frac{-E^* \cos\delta_i + V_o}{n_{iC} \cos\delta_i + \frac{Z_{oi}}{V_o}} \tag{35}$$

Substituting Equation (35) into (34), the deviation in voltage amplitude between two inverters is given by

$$\Delta E = E_1 - E_2 = \frac{-E^* \cos\delta_1 + V_o}{\cos\delta_1 + \frac{Z_{o1}}{n_{1C} V_o}} - \frac{-E^* \cos\delta_2 + V_o}{\cos\delta_2 + \frac{Z_{o2}}{n_{2C} V_o}} \tag{36}$$

Voltage deviation between two units leads to considerable error in power sharing. Therefore, in order for $n_{1C}Q_1 = n_{2C}Q_2$ to hold, the voltage deviation should be zero. However, this condition is not obeyed in practicality. It is satisfied if

$$\frac{n_{1C}}{Z_{01}} = \frac{n_{2C}}{Z_{02}} \text{ and } \delta_1 = \delta_2 \tag{37}$$

Therefore, in order to obtain accurate reactive power sharing, capacitive output impedance, $Z_o$ should be designed to satisfy the condition stated in Equation (38)

$$\frac{\mathrm{Z_{02}}}{\mathrm{Z_{01}}} = \frac{n_{2C}}{n_{1C}} = \frac{S_1}{S_2} \tag{38}$$

or

$$\frac{\mathrm{Z_{02}}S_2}{(\mathrm{E^*})^2} = \frac{\mathrm{Z_{01}}S_1}{(\mathrm{E^*})^2} \cdots \frac{\mathrm{Z_{0n}}S_n}{(\mathrm{E^*})^2} \tag{39}$$

where $S_1$, $S_2$, …, $S_n$ are inverter ratings in volt amperes. By referring to Equation (39), it is evident that for achieving accurate reactive power sharing, the p.u. output impedances of inverters should be the same, and this is the foundation of the approach known as virtual impedance. However, it is difficult to achieve this in a real scenario [7,14]. In the same way, it can be shown that real power sharing can be ensured under the condition of $\frac{\mathrm{Z_{02}}}{\mathrm{Z_{01}}} = \frac{m_{2C}}{m_{1C}}$.

### 3.2.2. Robust Droop Controller

As stated in Section 3.2.1, the conventional droop control strategy may not able to share power accurately due to the lack of a mechanism to ensure that voltage set points are the same under disturbance, noise, *etc.* [7,11,14]. This issue can be resolved through bolting a voltage regulator onto the conventional droop controller (CDC), as shown in Figure 8.

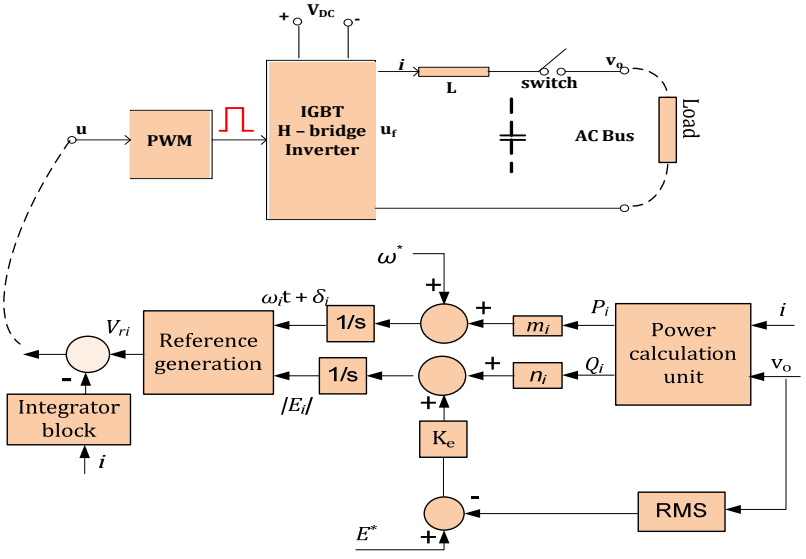



**Figure 8.** Robust droop controller for capacitive inverter.

At the steady state, input to the integrator is zero.

$$n_i \mathrm{Q}_i + \mathrm{K_e}\,(\mathrm{E^*} - \mathrm{V_o}) = 0 \tag{40}$$

If $K_e$ is same for all inverters that are operating in parallel, an accurate reactive power sharing is guaranteed in proportion to the power rating of the inverters.

$$\text{Thus, } n_i \mathrm{Q}_i = \text{constant} \tag{41}$$

By referring Equation (40), the output voltage, $\mathrm{V_o}$ is expressed as

$$V_o = E^* + \frac{n_i Q_i}{K_e} = E^* + \frac{n_i Q_i}{E^* K_e} E^* \quad (42)$$

The output voltage can be maintained within a desired range by choosing large $K_e$ thus achieving good voltage regulation.

### 3.2.3. Modification in Voltage Power Droop Characteristics

To speed up the dynamic response of power sharing, so that the input to an integrator becomes zero at the steady state, a proportional controller is added with it, as shown in Equation (43).

$$(n_{ci} Q_i + K_e (E^* - V_o)) (sK_p + 1) = sE_i \quad (43)$$

$$s\, n_{ci} Q_i K_p + s\, K_e (E^* - V_o) K_p + (n_{ci} Q_i + K_e (E^* - V_o)) = sE_i \quad (44)$$

or equivalently, the time domain form of Equation (44) is expressed as

$$n_{ci} K_p \frac{d}{dt} Q_i + K_e K_p \frac{d}{dt} (E^* - V_o) + (n_{ci} Q_i + K_e (E^* - V_o)) = \frac{d}{dt} E_i \quad (45)$$

The following structure, shown in Figure 9 can be drawn by referring Equation (45).

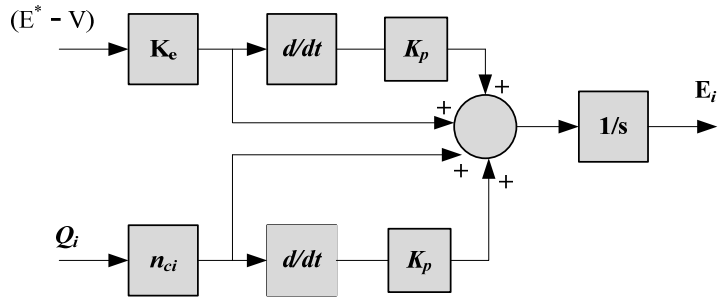



**Figure 9.** Equivalent diagram derived from Equation (45).

The value of $K_p$ is chosen carefully in order to get a stable response. In this study, the value of $K_p$ is chosen 0.4 for the linear load and 0.1 for the nonlinear load.

## 4. Bypassing Harmonic Current Strategy (BHC)

With the exception of capacitive inverters, when the load is nonlinear, the $THD_v$ is significant. The strategy of bypassing harmonic current components, shown in Figure 10, can be used to improve the quality of the output voltage. Generally speaking, nonlinear loads or/and pulse width modulation cause harmonic components in the current $i$ (shown in Figure 3), which cause harmonic voltage drops in the output impedance, $Z_o$. The output voltage quality degrades and causes high THD due to the appearance of harmonic voltage drops on the $Z_o$. Therefore, rather than its type, the output impedance value has a significant impact on $THD_v$ [7,12,13].

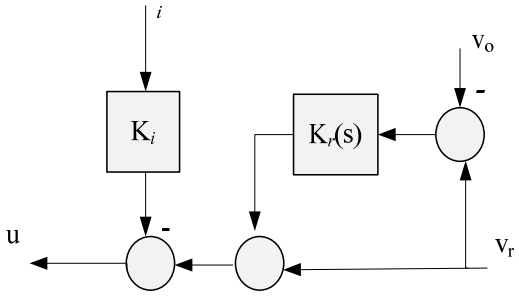



**Figure 10.** Controller for improvement in Voltage THD.

The output impedance of the inverter with this scheme is stated in Equation (46).

$$Z_o(s) = \frac{sL + K_i}{1 + K_r(s)} \tag{46}$$

where,

$$K_r(s) = \sum_{h=3,5,7} \frac{2\xi h\omega s}{(h\omega)^2 + 2\xi h\omega s + s^2} K_h \tag{47}$$

The $K_r(s)$ can be designed to have low gain at low frequency and high gain at high frequency to meet the requirements of power sharing and low output $THD_v$. This concept can be applied to all types of inverters. The following set of equations is written by referring to Figure 10.

$$u = v_r - K_i i + K_r(s)\,(v_r - v_o) \tag{48}$$

$$u = v_r + K_r(s)\,v_r - K_i i - v_o K_r(s) \tag{49}$$

$$u = v_r(1 + K_r(s)) - (v_o K_r(s) + K_i i) \tag{50}$$

$$u = v_r(1 + K_r(s)) - K_i i_L \tag{51}$$

where $i_L = i + \frac{K_r(s)}{K_i} v_o$

By referring Equation (51), it can be seen that the controller block of Figure 11 is equivalent to feedback current $i_L = i + \frac{K_r(s)}{K_i} v_o$, which is the summation of current through the admittance branch connected across the output terminals and $i$. In other words, it can be inferred that the block diagram shown in Figure 10 is equivalent to the controller block shown in Figure 11. After careful investigation, it can be seen that structurally the principle is the same as that of proportional current feedback control to achieve a resistive type inverter, with the exception of an additional current component of $\frac{K_r(s)}{K_i} v_o$ in inductor current, $i_L$. Filter capacitor C and admittance branch $\frac{K_r(s)}{K_i}$ form a parallel connection. In simple words, the controller block diagram of Figure 3 is equivalent to adding $\frac{K_r(s)}{K_i}$ with the filter capacitor, as shown in Figure 12.

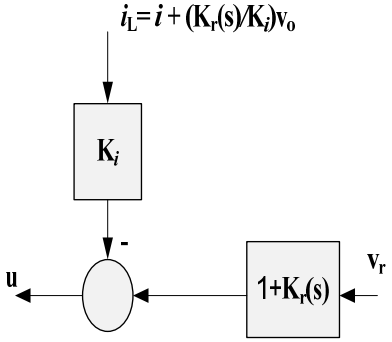



**Figure 11.** Equivalent block diagram.

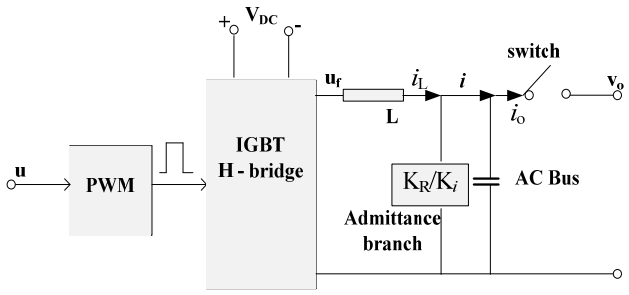



**Figure 12.** Equivalent circuit.

$$\frac{\mathrm{K}_r(s)}{\mathrm{K}_i} = \sum_{h=3,5\ldots} \frac{2\xi h\omega s}{s^2 + 2\xi h\omega s + (h\omega)^2} \frac{\mathrm{K}_h}{\mathrm{K}_i} \tag{52}$$

$$\frac{2\xi h\omega s}{s^2 + 2\xi h\omega s + (h\omega)^2} \frac{\mathrm{K}_h}{\mathrm{K}_i} = \frac{1}{\frac{s\,\mathrm{K}_i}{2\xi h\omega \mathrm{K}_h} + \frac{\mathrm{K}_i}{\mathrm{K}_h} + \frac{\mathrm{K}_i h\omega}{\mathrm{K}_h 2\xi s}} \tag{53}$$

There are parallel admittance branches corresponding to each harmonic frequency component. For example, if only two harmonic frequency components $h = 3$ and $h = 5$ are considered, then there will be a parallel combination of two admittance branches in the equivalent circuit diagram. Each branch is a series combination of resistance $\frac{\mathrm{K}_i}{\mathrm{K}_h}$, inductance $\frac{\mathrm{K}_i}{2\xi h\omega \mathrm{K}_h}$ and capacitance $\frac{2\xi \mathrm{K}_h}{h\omega \mathrm{K}_i}$, that resonates at the $h$-th harmonic frequency, *i.e.*, $h\omega$. This is illustrated in Figure 13.

Where $r_h = \frac{\mathrm{K}_i}{\mathrm{K}_h}$, $c_h = \frac{2\xi \mathrm{K}_h}{h\omega \mathrm{K}_i}$, $l_h = \frac{\mathrm{K}_i}{2\xi h\omega \mathrm{K}_h}$

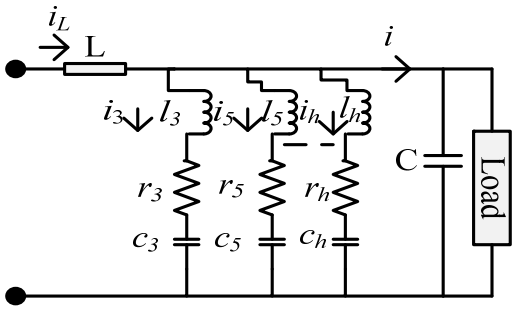



**Figure 13.** Individual harmonic currents through admittance branches.

It is worthwhile to note that $\frac{\mathrm{K}_i}{\mathrm{K}_h}$ is the remaining impedance (referring Equation (53)) at the $h$-th harmonic frequency. For completely eliminating the $h$-th harmonic voltage component in the output voltage, $\mathrm{K}_i$ should be zero because $\mathrm{K}_h$ is finite. This means that the resistive output impedance of the inverter adds the harmonics in the output voltage. It is possible to reduce some harmonic voltage components through a trade-off when determining $\mathrm{K}_i$.

In order to further improve the output voltage quality, the aforementioned strategy is modified. The modified strategy consists of multiple parallel circuits tuned to individual harmonic frequency components ($h = 3, 5, 7, \ldots$, *etc.*) as shown in Figure 14.

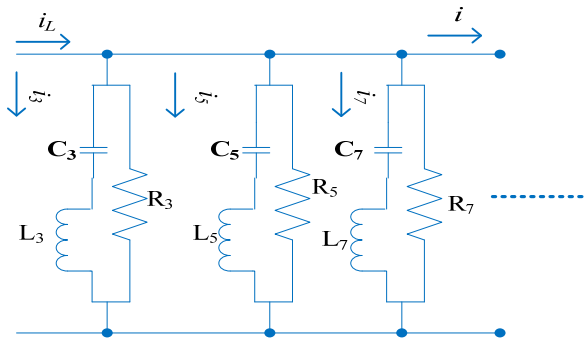



**Figure 14.** Shunt resonant filters in the proposed strategy.

Where $i_L$ is the filter inductor current, $i$ is the output current, and $i_h$ ($h$ = 3, 5, 7, ...) is the bypassed harmonic component of the current $i_L$. The $i_h$ is expressed as

$$i_h = \mathrm{v_o} Y_h \ (h = 3, 5, 7, \ldots) \tag{54}$$

where $Y_h$ is admittance of $h$-th circuit, expressed in Equation (55).

$$Y_h = \frac{L_h C_h s^2 + 1 + R_h C_h s}{R_h (L_h C_h s^2 + 1)} \tag{55}$$

The resonant frequency of the circuit tuned at $h$-th harmonic frequency is

$$\omega_h = \frac{1}{h\sqrt{L_h C_h}} \tag{56}$$

Now, the inductor current $i_L$ is

$$i_L = i + \mathrm{v_o} \sum_{h=3,5,7\ldots} \left(\frac{1}{Y_h}\right) \tag{57}$$

It is observed through Equation (55) that a circuit tuned at $h$-th harmonic frequency offers an infinite admittance path to the corresponding harmonic frequency current component, thereby bypassing it. In this way, the output voltage quality improves when harmonic current components bypass through tuned parallel circuits. Another way to look at this improvement is in terms of the output impedance of the inverter, which is derived as follows.

The following KVL equation can be written for the filter circuit of the inverter.

$$\mathrm{u} = \mathrm{sL} i_L + \mathrm{v_o} \tag{58}$$

L is a filter inductor in units of henry; $i_L$ is current through it and $\mathrm{v_o}$ is the output voltage.

The signal u, generated through the control strategy, is expressed as

$$\mathrm{u} = \mathrm{v_r} - \mathrm{K}_i i + \mathrm{Y}_r(\mathrm{s}) \ (\mathrm{v_r} - \mathrm{v_o}) \tag{59}$$

where $\mathrm{K}_i$ is the virtual resistance; $\mathrm{Y}_r$ is a virtual resonant admittance function; $\mathrm{v_r}$ is the reference voltage generated in the control scheme.

Upon equating signals in Equations (58) and (59).

$$\mathrm{v_r} - \mathrm{K}_i i + \mathrm{Y}_r(\mathrm{s}) \ (\mathrm{v_r} - \mathrm{v_o}) = \mathrm{sL} i_L + \mathrm{v_o}$$

$$\mathrm{v_o} = \mathrm{v_r} - \frac{s\mathrm{L} + \mathrm{K}_i}{1 + \mathrm{Y}_r(\mathrm{s})} i_L \tag{60}$$

The output impedance is expressed in Equation (61).

$$Z_o = \frac{s\mathrm{L} + \mathrm{K}_i}{1 + \mathrm{Y}_r(\mathrm{s})} \tag{61}$$

The magnitude and phase plots of $Z_o$ are shown in Figure 15.

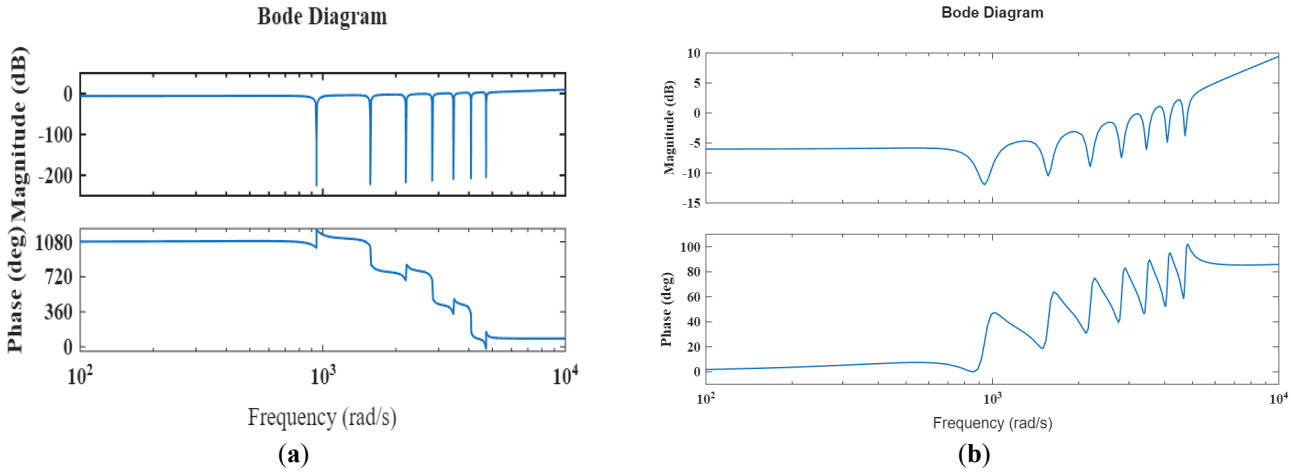



**Figure 15.** Magnitude and phase plot of $Z_o$ (**a**) with $r_{par}$ = 0, (**b**) with $r_{par}$ = 0.1 Ω.

The magnitude plot, shown in Figure 15a, reveals that the output impedance of the inverter at dominating harmonic frequencies ($h$ = 3, 5, 7, 9, 11, 13, 15) is close to zero. Therefore, the voltage drop at these harmonic frequencies also tends to zero, thereby improving the quality of the output voltage. By carefully examining Equation (55), it is observed that the phase value near these frequencies may not acquire zero value if parameters are not tuned properly, leading to instability in the system. In order to overcome this, a small parasitic resistance $r_{par}$ (≈0.1 Ω) is considered in series with $L_h$.

With this consideration, the magnitude and phase plots are shown in Figure 15b. The admittance at $h$-th harmonic frequency is $\frac{R_h + r_{par}}{r_{par}\, R_h}$.

## 5. Stability Analysis

In this section, the small signal stability analysis for the inverter control system of capacitive inverter and resistive inverter (BHC strategy) is discussed [14].

### *5.1. Small Signal Stability Analysis*

The small signal stability analysis of the capacitive inverter system is described in the following subsection. Subsequently, the simulation results of various scenarios are discussed.

Small signal stability is conducted for one inverter participating in the parallel operation. Small disturbances around the phase angle (δ) and the inverter RMS voltage (E) are considered when linearizing Equation (31). $V_o$ is the RMS output voltage across the load.

$$\Delta P(\mathrm{s}) = V_o \frac{(\cos\delta\cos\theta + \sin\delta\sin\theta)}{Z_o}\Delta E(\mathrm{s}) + \frac{E\,V_o(-\sin\delta\cos\theta + \cos\delta\sin\theta)}{Z_o}\Delta\delta(\mathrm{s}) \tag{62}$$

$$\Delta Q(\mathrm{s}) = V_o \frac{(\cos\delta\sin\theta - \sin\delta\cos\theta)}{Z_o}\Delta E(\mathrm{s}) - \frac{EV_o\,(\sin\delta\sin\theta + \cos\delta\cos\theta)}{Z_o}\Delta\delta(\mathrm{s}) \tag{63}$$

Linearizing controller Equations in Equation (34) yields

$$\mathrm{s}\Delta E(\mathrm{s}) = n_C\Delta Q(\mathrm{s}) \tag{64}$$

$$\Delta\omega(\mathrm{s}) = m_C\Delta P(\mathrm{s}) \text{ and } \Delta\omega(\mathrm{s}) = \mathrm{s}\Delta\delta(\mathrm{s}) \tag{65}$$

Normally, the powers (Active & Reactive) are measured through low pass filter of the form $\frac{\omega_f}{s + \omega_f}$. Considering this and using Equations (62)–(65), a fourth order polynomial is formed in 's' to investigate

the stability (refer to Appendix A). It is evident from Figure 16a that the proposed strategy is stable for output impedance angle ranging from $-\frac{\pi}{2}$ to 0 radians.

Now, when proportional gain ($K_p$) is added around an integrator in the voltage-active power loop, the following variables are chosen as states.

$$X = [P\ Q\ E\ \delta\ V_o\ E_{ref}\ V_c]^{\mathrm{T}} \tag{66}$$

$$P = -(E_{ref} - V_c)\ V_o \sin(\delta)/Z_o \tag{67}$$

$$Q = (-(E_{ref} - V_c)\ V_o \cos(\delta) + V_o^2)/Z_o \tag{68}$$

$$E = \int (n_C \mathrm{Q} + K_e(E^* - V_o))dt \tag{69}$$

$$\frac{d}{dt}\delta = m_C \Delta P \tag{70}$$

$$C\frac{d}{dt}V_o = i_L - i_o \tag{71}$$

$$\frac{d}{dt}i_L = \frac{1}{L}(E_{ref} - V_c - V_o) \tag{72}$$

$$E_{ref} = E + K_p\ (n_C \mathrm{Q} + K_e(E^* - V_o)) \tag{73}$$

$$V_c = \frac{1}{C_o}\int i_L\ dt \tag{74}$$

where $E_{ref}$ and $V_c$ are the RMS value of reference voltage and voltage across the virtual capacitor, respectively. The taylor expansion of the dynamic model, presented in Equations (66)–(74) yields the small signal model with the following state space equation.

$$\dot{X} = A_s \mathrm{X} \tag{75}$$

where,

$$\dot{X} = [\dot{P}\ \dot{Q}\ \dot{E}\ \dot{\delta}\ \dot{V_o} i_L^{\cdot}\ \dot{E_{ref}}\ \dot{V_c}] \tag{76}$$

$$\dot{X} = \frac{d}{dt}X \tag{77}$$

The coefficients of the state space matrix, $A_s$, are not expressed here due to the page limit. In order to access the effect of $K_p$ on the system damping, the eigenvalues are computed for two cases as shown in Tables 2 and 3 below.

**Table 2.** Eigenvalues, $K_p = 0$.

| Sr No. | Eigenvalues |
|---|---|
| 1 | $-2340.271717 + 3666.498711i$ |
| 2 | $-2340.271717 - 3666.498711i$ |
| 3 | −369.9716286 |
| 4 | −9.149825932 |
| 5 | −9.989995299 |
| 6 | −0.8501672472 |
| 7 | $1.190287144 \times 10^{-13}$ |
| 8 | 0 |

**Table 3.** Eigenvalues, $K_p$ = 0.035.

| Sr No. | Eigenvalues |
|---|---|
| 1 | $-2420.110132 + 5226.538233i$ |
| 2 | $-2420.110132 - 5226.538233i$ |
| 3 | $-210.8111876$ |
| 4 | $-9.980771261$ |
| 5 | $-10.01468126$ |
| 6 | $-0.01922682259$ |
| 7 | $-0.2048357311 + 0.7534399889i$ |
| 8 | $-0.2048357311 - 0.7534399889i$ |

In Table 2, two very slow decaying modes (7th: $1.190287144 \times 10^{-13}$ and 8th: 0) are shown, which shift to the left side of the complex plane upon adding the proportional gain ($K_p$) as shown in Table 3. If $K_p$ increases beyond certain value, system will lose its stability. The traces of dominant eigenvalue with respect to increasing $K_p$ are shown in Figure 16b.

Further, a PF (participation factor) based analysis is conducted, illustrated in Table 4, to notice the participation of various states in a particular eigenvalue.

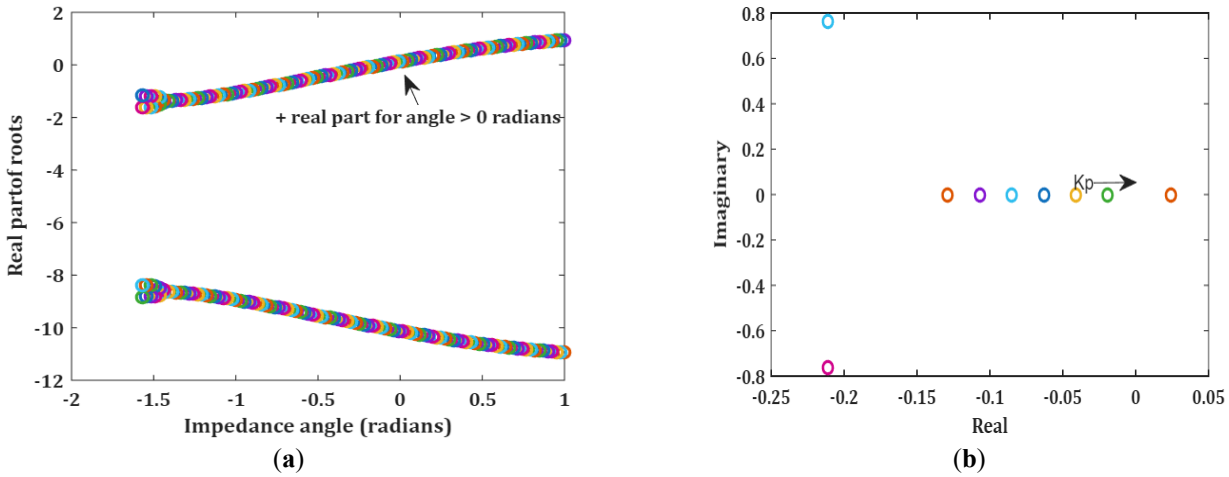



**Figure 16.** (**a**) Characteristics of roots *vs*. inverter output impedance angle; (**b**) Traces of dominant eigenvalue.

**Table 4.** Participation factor based analysis.

| State No. \ Mode No. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| **1** | 0 | 0 | 0 | 1.0018 | 0.0001 | 0.0019 | 0 | 0 |
| **2** | 0 | 0 | 0.0001 | 0.0001 | 1.0386 | 0 | 0.0415 | 0.0415 |
| **3** | 0 | 0 | 0.0001 | 0 | 0.1289 | 0 | 0.8893 | 0.8893 |
| **4** | 0 | 0 | 0 | 0.0019 | 0 | 1.0019 | 0 | 0 |
| **5** | 0.4408 | 0.4408 | 0.4625 | 0 | 0.0019 | 0 | 0.0014 | 0.0014 |
| **6** | 0.5681 | 0.5681 | 0.0316 | 0 | 0 | 0 | 0 | 0 |
| **7** | 0.2278 | 0.2278 | 0.3645 | 0 | 0.0892 | 0 | 0.8478 | 0.8478 |
| **8** | 0.0224 | 0.0224 | 0.9333 | 0 | 0.0029 | 0 | 0.0286 | 0.0286 |

It is observed that there is a heavy dominance of states $E$ and $V_{ref}$ in eigenvalues 7th and 8th. Similarly, 4th eigenvalue is dominated by state $\dot{P}$. Eigenvalue pair-1,2 is dominated by states 5–8 primarily.

### *5.2. Interpretation*

For a stable system, participation factor analysis provides the physical interpretation of the stable modes by identifying the dominant state variables associated with each eigenvalue. This enables classification of the system dynamics and indicates the controller states whose parameters are the most effective for improving damping or modifying dynamic performance, even when all eigenvalues lie in the left-half of the complex plane.

### *5.3. Stability Analysis (BHC Strategy)*

The inductor current, as stated in Equation (78), is the sum of the currents through the load and the filter capacitor.

$$i = (\frac{1}{Z_L} + \frac{sC}{srC + 1})\mathrm{v_o} \tag{78}$$

where $r_{esr}$ is the equivalent series resistor of the filter capacitor. The Equation (78) can also be written as in Equation (79).

$$i = \frac{\mathrm{v_o}}{Z_{eqv}} \tag{79}$$

$Z_{eqv}$ is the equivalent impedance of the parallel combination of the filter capacitor and the load as shown in Figure 17a. If load $Z_L$ is passive, then it must be a positive real function, the equivalent impedance $Z_{eqv}$ is stable for any passive $Z_L$ as Nyquist plot of open loop transfer function $\frac{1}{Z_L}\frac{srC+1}{sC}$, shown in Figure 17b, does not encircle the critical point (−1,0) on the s plane. It is noticeable that the presence of equivalent series resistance $r$ guarantees the system stability as it suppresses the oscillations. The stability of the closed loop transfer function can be judged by drawing the nyquist diagram of function M(s), described in Equation (80). However, if the controller is implemented digitally, the open loop transfer function is modified to $\frac{(1+\mathrm{K_r(s)}e^{-T_s s})}{sL+K_i e^{-T_s s}} Z_{eqv}$, where $T_s$ is the sampling period. Now, the proportional gain has to follow the inequality $K_i < \frac{\pi}{2}\frac{\mathrm{L}}{T_s}$ for ensuring the system stability.

$$\mathrm{M(s)} = \frac{1+\mathrm{K_r(s)}}{sL+K_i} Z_{eqv} \tag{80}$$

where,

$$Z_{eqv} = \frac{Z(s)}{1+\frac{Z(s)}{Z_L(s)}} \tag{81}$$

and,

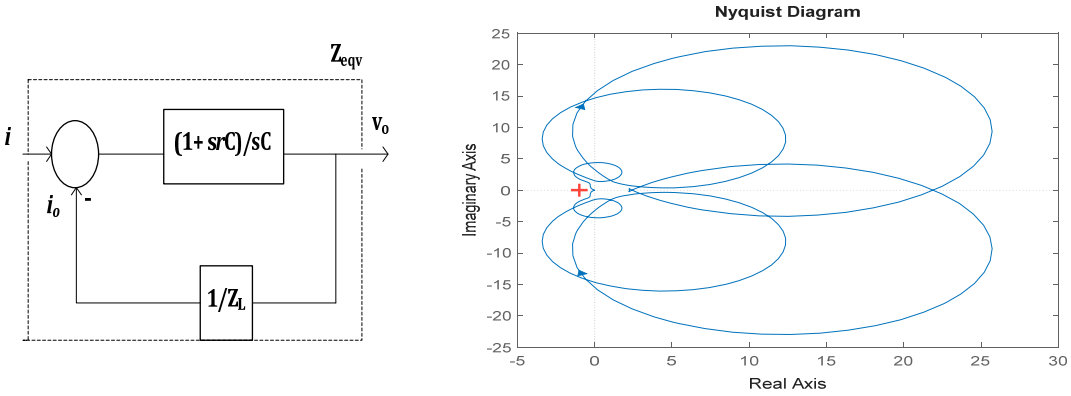
$$Z(s) = \frac{1+srC}{sC} \tag{82}$$

$$Z_L = \frac{v_o}{i_o} \tag{83}$$

The finite parameter $\mathrm{K_h}$ in the controller can be determined by using the stability condition of small gain theorem. According to this theorem, system is stable if $\left\|\frac{1+K_R(s)}{sL+K_i} Z_{eqv}\right\|_{\infty} < 1$, where $\left\|\frac{1+K_R(s)}{sL+K_i} Z_{eqv}\right\|_{\infty}$ is the maximum amplitude of open loop transfer function M(s).

In order to determine the upper limit of $\mathrm{K_3}$, bode plots of M(s) are drawn in Figure 18 for $\mathrm{K_3}$ = 15, 40, and 65, respectively. By careful observation of these plots, it is revealed that the system is stable for $\mathrm{K_3}$ = 15 as peak magnitude is less than 1 in linear scale, whereas it approaches 1 for $\mathrm{K_3} \approx 40$. The system is not stable for $\mathrm{K_3}$ = 65 as peak magnitude is more than 1. Therefore, the upper limit for $\mathrm{K_3}$ is determined by

using the stability criteria of small gain theorem. Similarly, the safe operating limits for $K_5$ and $K_7$ can also be determined.




(**a**) (**b**)

**Figure 17.** (**a**) Equivalent impedance $Z_{eqv}$; (**b**) Nyquist plot of open loop system.

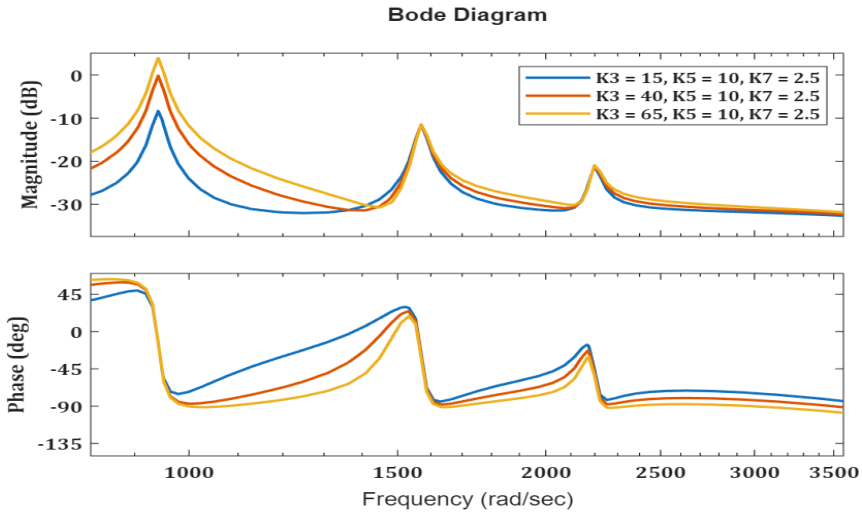
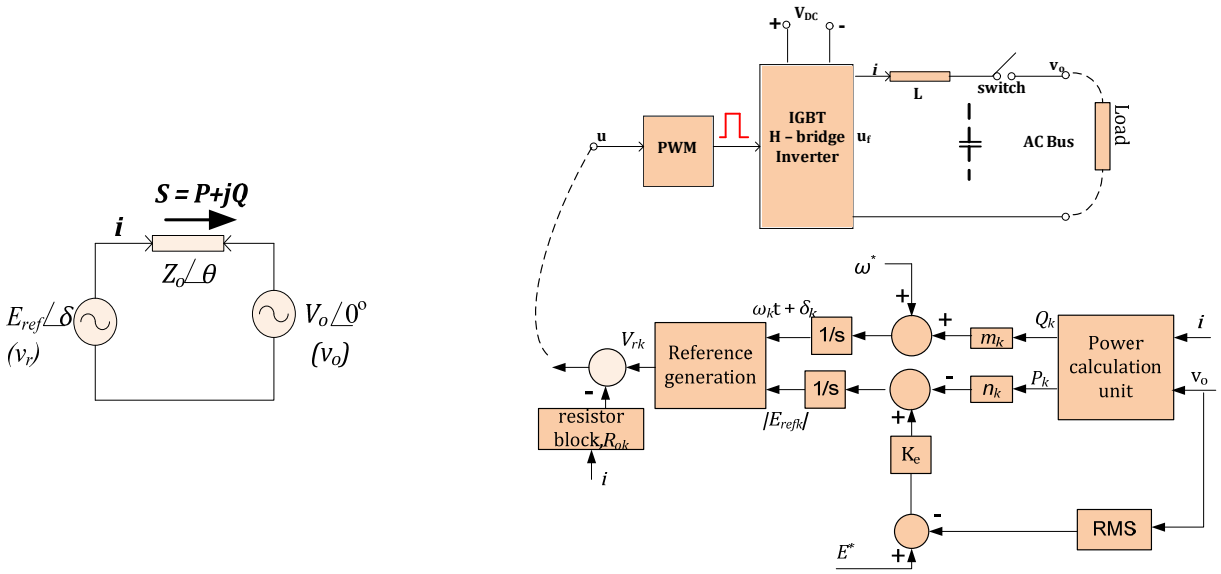



**Figure 18.** Bode diagram for M(s).

## 6. Power Sharing in Resistive Inverters (BHC)

### *6.1. Real Power Sharing*

The real and reactive power, shown in Figure 19a, supplied by an individual inverter *k*, are stated in Equations (84) and (85) [7,10,11,13,14].




**(a)** **(b)**

**Figure 19.** (**a**) Inverter model; (**b**) resistive type inverter equipped with robust droop control

Due to feedback resistive block, output impedance of inverter is dominantly resistive. Under this condition, $Z_{ok} = R_{ok}$,

$$P_k = \left(\frac{E_{refk}V_o}{R_{ok}} cos(\delta_k) - \frac{V_o^2}{R_{ok}}\right) \tag{84}$$

$$Q_k = -\frac{E_{refk}V_o}{R_{ok}} sin(\delta_k) \tag{85}$$

Therefore, the CDC for resistive inverter takes the form

$$E_{refk} = -n_k P_k + E^* \tag{86}$$

$$\omega_k = m_k Q_k + \omega^*$$

where,

$E_{refk}$: magnitude of reference voltage (volt) of $k$-th inverter

$\delta$: phase angle of the reference voltage (radians)

$|Z_{ok}|$: magnitude of $Z_{ok}$ ($\approx R_{ok}$) ($\Omega$)

$\theta$: angle of $Z_o$ (radians)

$S$, $P$ and $Q$: apparent, real and reactive power (VA, W and VAr)

$i$: current flowing through $Z_o(R_o + j\,X_o)$ (amp)

$V_o$: voltage of output terminals (volt)

$E^*$ and $\omega^*$ are nominal voltage and frequency of the system.

$n_k$ and $m_k$ are droop coefficients, which are computed through voltage drop ratio ($\frac{n_k P_k}{E^* K_e}$) and frequency boost ratio ($\frac{m_k Q_k}{\omega^*}$) respectively.

Referring Equations (84) and (86), the expression of active power of inverter $k$ is expressed as

$$P_k = \frac{E^* cos\delta_k - V_o}{n_k\, cos\delta_k + \frac{R_{ok}}{V_o}} \tag{87}$$

By referring Equations (86) and (87), the deviation of voltage amplitude ($\Delta E$) between two inverters is expressed in Equation (88).

$$\Delta E = E_{ref2} - E_{ref1} = \frac{E^* cos\delta_1 - V_O}{cos\delta_1 + \frac{R_{o1}}{n_1 V_o}} - \frac{E^* cos\delta_2 - V_O}{cos\delta_2 + \frac{R_{o2}}{n_2 V_o}} \tag{88}$$

The deviation in the voltage between two units lead to a significant error in power distribution. Therefore, in order for $n_1P_1 = n_2P_2$ to hold, $\Delta E$ should be zero. However, this condition is not fulfilled in practicality. It is fulfilled if

$$\frac{n_1}{R_{o1}} = \frac{n_2}{R_{o2}} \text{ and } \delta_1 = \delta_2 \tag{89}$$

Therefore, for achieving accurate active power sharing, resistive output impedances ($R_{ok}$, $k$ = 1, 2) of two inverters should be designed to satisfy

$$\frac{R_{02}}{R_{01}} = \frac{n_2}{n_1} = \frac{S_1}{S_2} \tag{90}$$

Referring to Equation (90), it is clear that the p.u. output impedances of inverters must be the same in order to achieve accurate real power sharing. This is the foundation of the virtual impedance method. However, in practicality, there are challenges to achieve [7].

### *6.2. Reactive Power Sharing*

In steady state operation of inverters, accuracy of reactive power sharing is guaranteed under the condition $\omega_1 = \omega_2$. This is equivalent to

$$m_1Q_1 = m_2Q_2 \tag{91}$$

Alternatively, $m_1 \frac{E_{ref1}V_o}{R_{01}} \sin\delta_1 = m_2 \frac{E_{ref2}V_o}{R_{o2}} \sin\delta_2$

Under the condition of $\delta_1 = \delta_2$ and $E_{ref1} = E_{ref2}$

$$\frac{R_{02}}{R_{01}} = \frac{m_2}{m_1} \tag{92}$$

The above analysis concludes that $n_k$ & $m_k$ are related to accurate proportional power sharing in the conventional droop controller. In practicality, it is difficult to achieve the same per unit output impedance for inverters participating in the parallel operation. Other than this, disturbance, noise, and drift in parameters also limit proportionate power sharing. The concept of robust droop control, discussed in the next subsection, can be used to address this issue.

### *6.3. Proportional Load Sharing*

The Physical implementation of single phase inverter with its control loop is shown in Figure 3. In the inverter control loop, the feedback integrator block is replaced by a pure resistance (also called a virtual resistor) while implementing the BHC strategy. The 1-Φ resistive inverter, equipped with RDC scheme, is shown in Figure 19b, to achieve proportional power sharing [11]. The RMS value of the output voltage is compared with the nominal system voltage, and this difference is amplified by a gain to produce a signal that is summed up in the power-voltage loop. An idea behind bolting a regulator loop needs to be understood for proportional power sharing. The voltage-power droop, expressed in Equation (86), can also be stated as follows

$$E_{refk} - E^* = \Delta E_k = -n_kP_k \tag{93}$$

Now,

$$E_{refk} = \int_0^t \Delta E_k \, dt \tag{94}$$

Equation (94) works well for the grid-tied mode, where $\Delta E_k$ must be zero as set power is sent to the grid without any error [11]. On the other hand, in off-grid mode, active power depends on the connected load and therefore $\Delta E_k$ may not be zero. It also means that controller has to be different for two different operating modes. However, to avoid this, the principle of basic control theory can be used, where $(E^* - V_o)$ is amplified and added to $\Delta E_k$ as shown in Figure 19b. This scheme is immune to computational errors, noise, and even disturbances. Additionally, this is a robust structure with respect to parameter drifts and component mismatches.

At the steady state, in power-voltage (*P*-*E*) loop, input to the integrator is zero.

$$n_k P_k - \mathrm{K_e}(E^* - V_o) = 0 \tag{95}$$

If $\mathrm{K_e}$ is same for all inverters that are operating in parallel, the accurate reactive power sharing is guaranteed in proportion to the power rating of the inverters. Hence,

$$n_k P_k = \text{constant} \tag{96}$$

Equation (96) justifies an accurate active power sharing without the need for the same reference voltages. Moreover, the sharing of power need not necessarily depend on feeder impedances.

By referring Equation (95), $V_o$ is expressed as

$$V_\mathrm{o} = E^* - \frac{n_k P_k}{\mathrm{K_e}} = E^* - \frac{n_k P_k}{E^* K_e} E^* \tag{97}$$

where $\frac{n_k P_k}{E^* \mathrm{K_e}}$ is the voltage drop ratio. $m_k$ and $n_k$ are computed via frequency boost ratio ($\frac{m_k \mathrm{Q}_k}{\omega^*}$) and voltage drop ratio, respectively.

Without bolting the regulator on the control loop of the inverter, the proportional power sharing between parallel inverters can not be guaranteed until the p.u. output impedances of inverter units are the same.

### *6.4. Voltage Regulation*

In the RDC model of inverter, the voltage drop ratio is smaller than the drop ratio due to load and/or droop component. On the other hand, the conventional droop controller includes the voltage drop ratio due to the droop component only and does not include the voltage drop ratio of the load component. Therefore, the discussed RDC scheme compensates for the voltage drop ratio due to load as well as the droop component and provides good capability of voltage regulation. According to Equation (97), the voltage drop ratio depends on $n_i$, $P_i$ and $\mathrm{K_e}$. Large $\mathrm{K_e}$ enables a much smaller voltage drop ratio. However, if the voltage measurement is erroneous, the trade off between power sharing accuracy and voltage drop must be made as the voltage drop is proportional to $\frac{n_i}{\mathrm{K_e}}$ and power sharing error is inversely proportional to $\frac{n_i}{\mathrm{K_e}}$. For an example, if an error in voltage measurement ($\frac{\Delta V_o}{E^*}$), which may be due to inaccurate sensor measurement, is 0.1% at the rated power and drop ratio ($\frac{n_i P_i}{\mathrm{E^* K_e}}$) is 5%, the error in active power sharing becomes $\frac{0.1}{5} = 2\%$, that is quite reasonable.

The deviation of output voltage from its nominal value is shown in Table 5, for capacitive and BHC assisted inverter.

**Table 5.** Steady state voltage deviation.

| **Strategy/Method** | $\frac{\lvert E^* - V_o \rvert}{E^*} \times 100$ |
|---|---|
| Capacitive type Inverter | 3.6 |
| BHC Controlled Inverter | 4 |

### *6.5. Need of Development in $Z_o$*

There is a further need of development in $Z_o$. This can be understood by taking an example of integral control assisted inverter. When it comes to the significant voltage harmonics at low frequencies, the overall output impedance is essentially the same as the output impedance without taking the filter capacitor into account. The ideal virtual capacitor $C_o$ is therefore largely unaffected by the filter capacitor. However, further research is required to investigate the impact of the filter capacitor on the overall performance of the inverter system.

By referring Figure 3 [12]

$$\mathrm{u} = \mathrm{v_r} - \frac{1}{sC_o} i \tag{98}$$

Also,

$$\mathrm{u_f} = (r + \mathrm{sL})i + \mathrm{v_o} \tag{99}$$

Therefore,

$$\mathrm{v_r} - \frac{1}{sC_o} i = \mathrm{sL}i + \mathrm{v_o} \tag{100}$$

where $i$ is summation of output current ($i_o$) and current through filter capacitor branch ($i_f = \frac{\mathrm{v_o}}{\frac{1}{sC} + r_{esr}}$).

Therefore,

$$\mathrm{v_o} = K_{vr}\mathrm{v_r} - Z_o i_o \tag{101}$$

where,

$$K_{vr} = \frac{\frac{1}{sC} + r_{esr}}{\frac{1}{sC} + r_{esr} + \frac{1}{sC_o} + r + \mathrm{sL}} \tag{102}$$

At low frequencies,

$$K_{vr} = \frac{1}{\frac{C}{C_o} + 1} \tag{103}$$

Normally, at the fundamental frequency, $C << C_o$

$$K_{vr} \approx 1$$

This means that $C$ and $r_{esr}$ have negligible impact on the output voltage at the fundamental frequency. Let us examine the effect of filter capacitor for the third harmonic voltage component. It is evident that when $C$ increases, the phase curve shifts to the left and the top of the magnitude curve shifts to the left-bottom (see Figure 20). If there are some harmonic components in the reference voltage $v_r$, it suggests that the filter capacitor affects voltage harmonics. The phase curve becomes smoother and the peak falls significantly as $r$ and $r_{esr}$ increases.

The virtual resistor can be added to the virtual resonant impedance to prevent energy loss brought on by the real resistor. On the one hand, the virtual resistor would increase the magnitude of voltage harmonic components throughout a broad frequency range. Conversely, it might reduce the magnitude of voltage harmonic components at the resonant frequencies of virtual resonant impedance. Additionally, the virtual resistor gives the system better stability and damping. Then, it is necessary to research how to carefully design parameters to reduce $\mathrm{THD_v}$ while retaining good damping.

Incorporating smartness in the output impedance is an another way to think in this direction. To overcome the limitations of tuned filters, smart impedance enables the removal of the need for tuning procedures and performs multiple-frequency harmonic mitigation electronically, *etc.* [20].

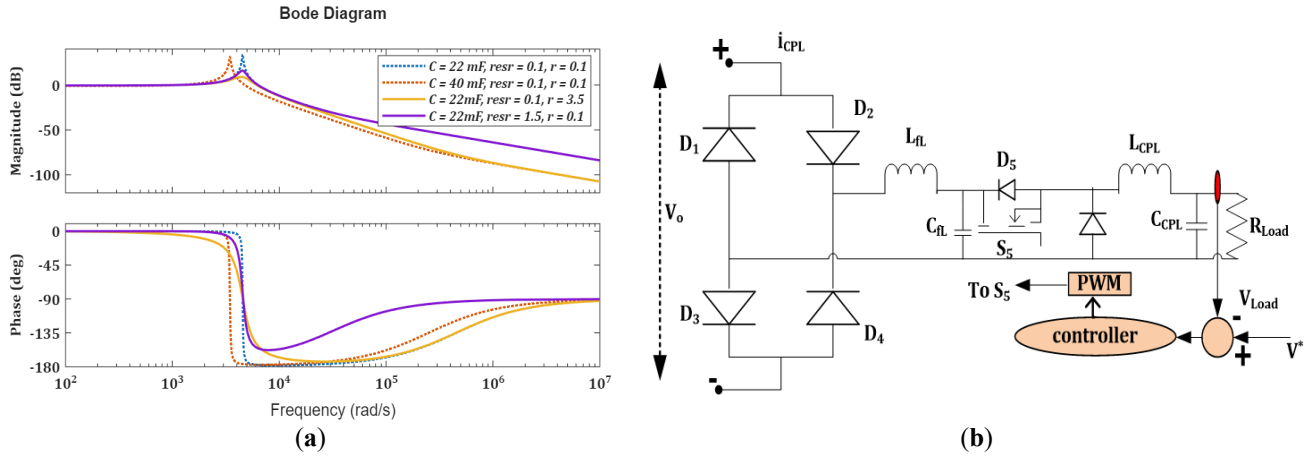



**Figure 20.** (**a**) Bode plot of $K_{vr}$; (**b**) Nonlinear load-2.

## 7. Result and Discussion

### *7.1. Capacitive Inverter Simulation with Linear Load*

A system of two single phase capacitive inverters operating in parallel is simulated for 10 s to verify the design. Matlab Simulink R2025b software is used to carry out simulations on the system with processor Intel (R) Core (TM) i5-8365U CPU @ 1.60GHz 1.90 GHz and 8 GB ram. Initially, inverter 1 (50 VA) and inverter 2 (25 VA) are operated in parallel to supply a linear load (R = 9 Ω). At $t$ = 4.5 s, inverter 2 (25 VA) stops operating, and inverter 1 (50 VA) alone shares the connected load. Detailed simulation parameters are given in Table 6.

**Table 6.** Detailed parameters.

| Parameters | Value | Unit |
|---|---|---|
| $F$ | 50 | Hz |
| $V_{DC}$ | 42 | V |
| $E^*$ | 12 | V |
| $f_s$ | 7500 | Hz |
| L (filter) | 2.35 | mH |
| $\omega^*$ | 314 | rad/s |
| $C$ (filter) | 22 | µF |
| $K_e$ | 20 | |
| $Z_L$ (Load) | 9 | Ω |
| $m_{1C}$ | 0.14 | rad/Watt |
| $m_{2C}$ | 0.07 | rad/Watt |
| $n_{1C}$ | 2.2 | V/var |
| $n_{2C}$ | 1.1 | V/var |
| $C_o$ | 325 | µF |

Time domain responses are shown in Figure 16. By referring Figure 21a, it is evident that both inverters share power (P) in the ratio of 1:2 ($\frac{5.26}{10.53} \approx \frac{1}{2}$) during parallel operation. In the same time interval, reactive power (Q) also settles in the ratio of 1:2 ($\frac{-0.6567}{-1.312} \approx \frac{1}{2}$). Inverter current and voltages are shown in Figure 21c–f.

The total load power is $\frac{E^{*2}}{R_L} = \frac{144}{9}$ = 16 Watt. The total power shared, when both INV1 and INV2 are operational, is 10.53 + 5.26 ≈ 15.8 Watt which is very close to 16 Watt.

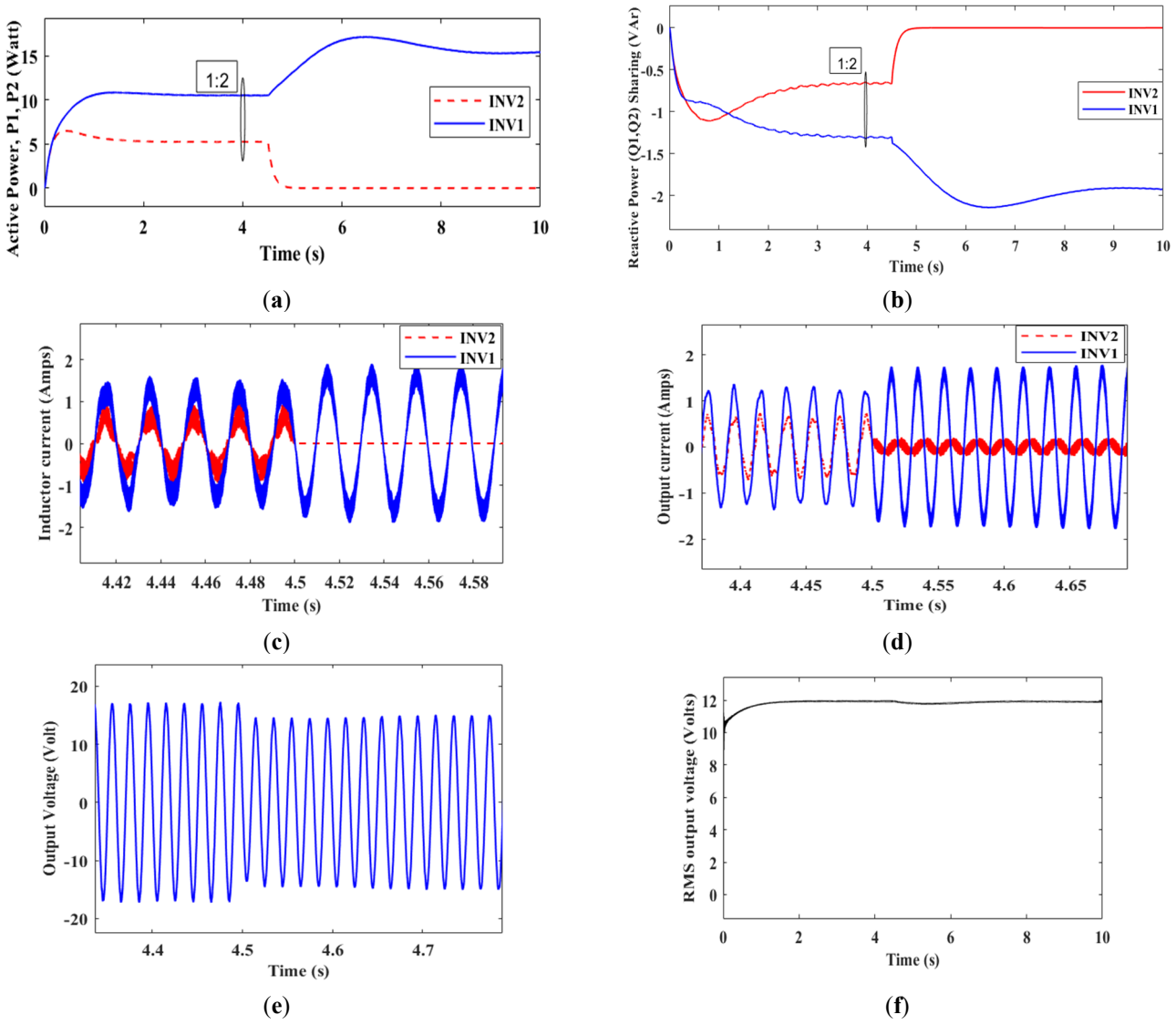



**Figure 21.** (**a**) Active power distribution *vs*. time; (**b**) Reactive power distribution *vs*. time; (**c**) Inductor current *vs*. time; (**d**) output current *vs*. time; (**e**) output voltage *vs*. time and (**f**) RMS output voltage *vs*. time.

## *7.2. Nonlinear Load*

(i) A system of two single phase capacitive inverters operating in parallel is simulated for 10 s to verify the design. Initially inverter 1 (50 VA) and Inverter 2 (25VA) are operated in parallel to feed a nonlinear load-1, $Z_L$ (full bridge rectifier with LC filter, $L_{NL}$ = 150 µH and $C_{NL}$ = 1000 µF, $R_{NL}$ = 9 Ω). At $t$ = 4.5 s, inverter-2 is disconnected and only inverter-1 is connected to the load. The simulation results are shown in Figure 22.

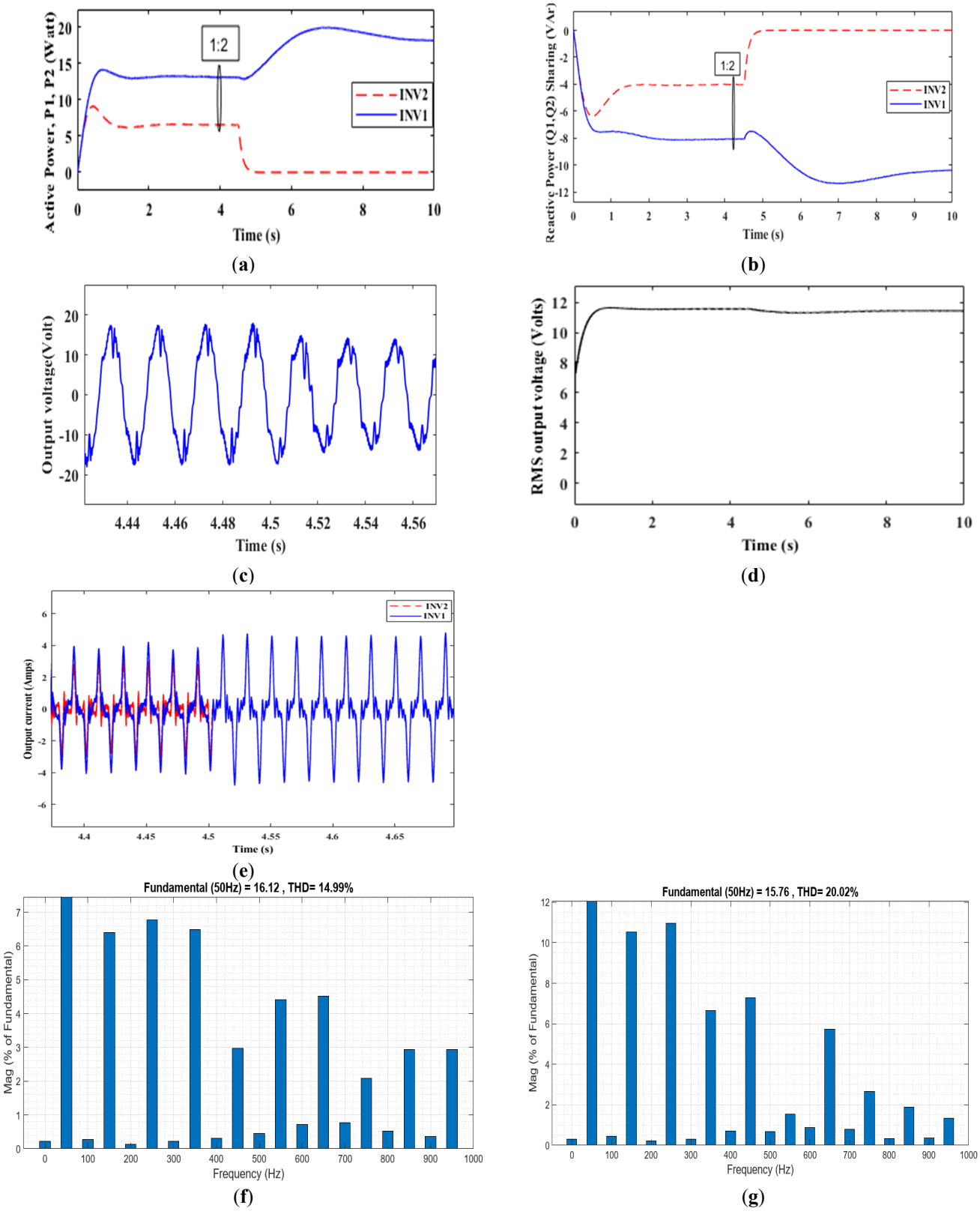



**Figure 22.** (**a**) Active power distribution *vs*. time; (**b**) Reactive power distribution *vs*. time; (**c**) output voltage *vs*. time; (**d**) RMS Output voltage *vs*. time; (**e**) output current *vs*. time; (**f**) % THD in load voltage when inverter 1 is operational; (**g**) %THD in load voltage when both inverters are operational.

(ii) The results, shown in Figure 23, are obtained by considering the structure discussed in Section 3.2.3. The rest of the parameters are the same as those taken for the nonlinear load case. The steady state values of variables are nearly same as that of scenario, discussed in Section 7.2.

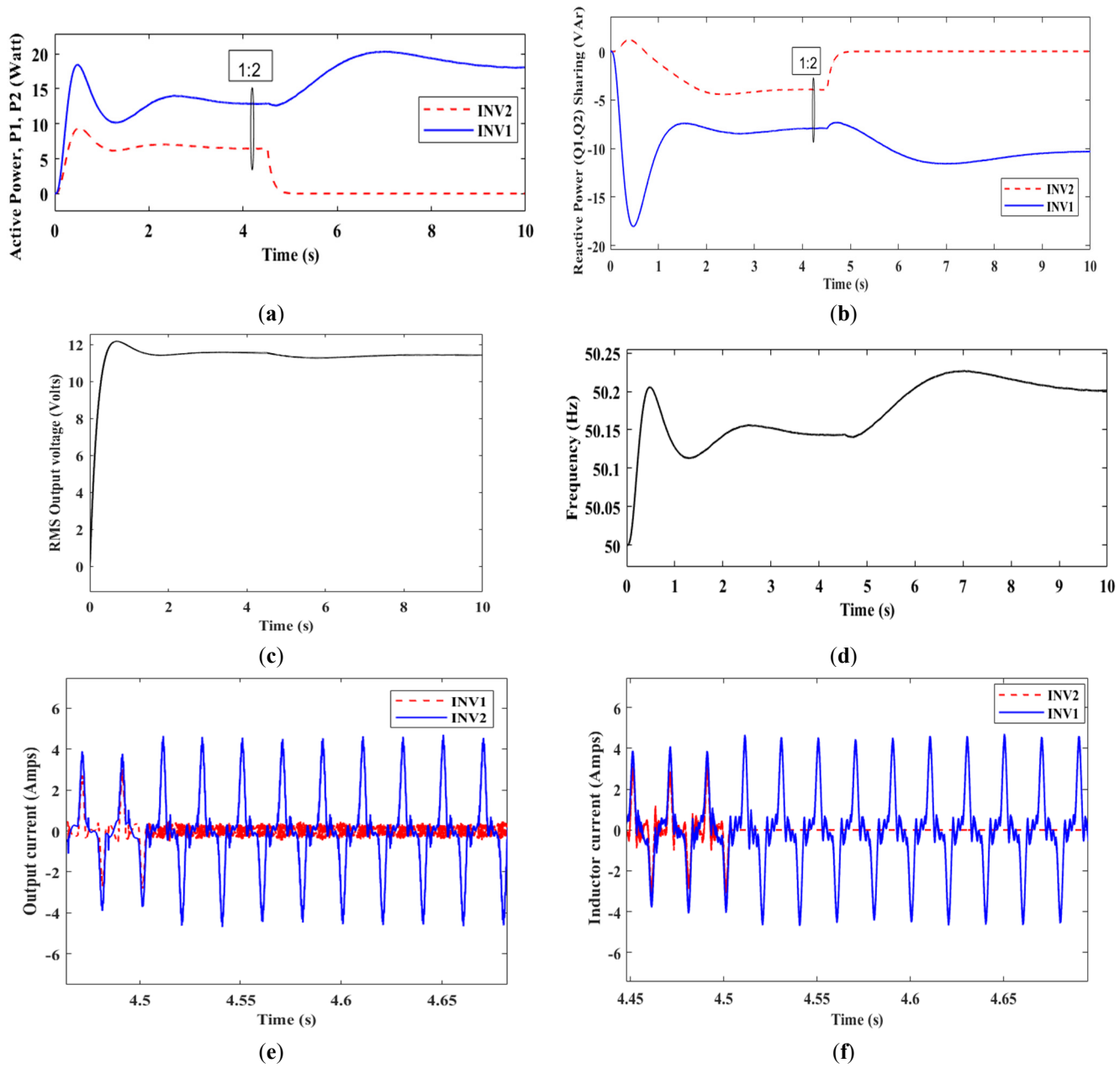



**Figure 23.** (**a**) Active power sharing *vs*. time; (**b**) Reactive power sharing *vs*. time; (**c**) RMS output voltage; (**d**) Frequency *vs*. time; (**e**) Output current *vs*. time and (**f**) inductor current *vs*. time.

### *7.3. Parallel Operation of Three Inverters*

One more similar inverter 3, which has VA rating one third of inverter 1, is added. The reactive power-voltage and active power-frequency coefficients ($n_{c3}$, $m_{c3}$), calculated from the voltage drop/boost ratio and the frequency drop/boost ratio respectively, are three times those of inverter 1. When all three inverters operate in parallel, at the steady state, the power sharing ratio between inverter-1 and inverter-2 is 2:1 ($\frac{10.79}{5.384} \approx \frac{2}{1}$), between inverter-1 and inverter-3 is 3:1 ($\frac{10.79}{3.603} \approx \frac{3}{1}$). The RMS output voltage, output voltage, output current, and inductor current are shown in Figure 24c–g, respectively. In Figure24d,e, waveforms $v_{o1}$, $v_{o2}$ and $v_{o3}$ appear identical, as expected, since they are measured at the common output terminals.

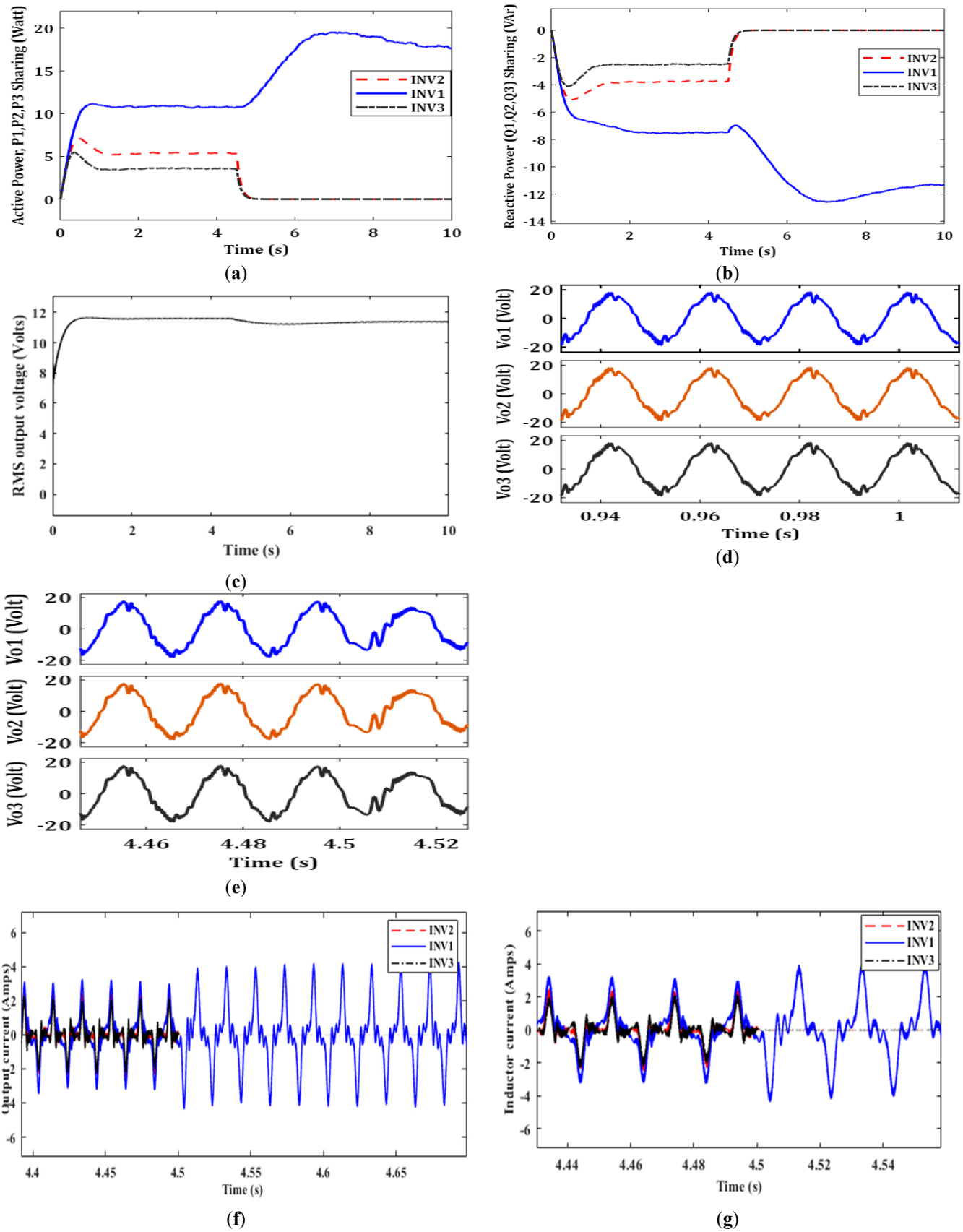


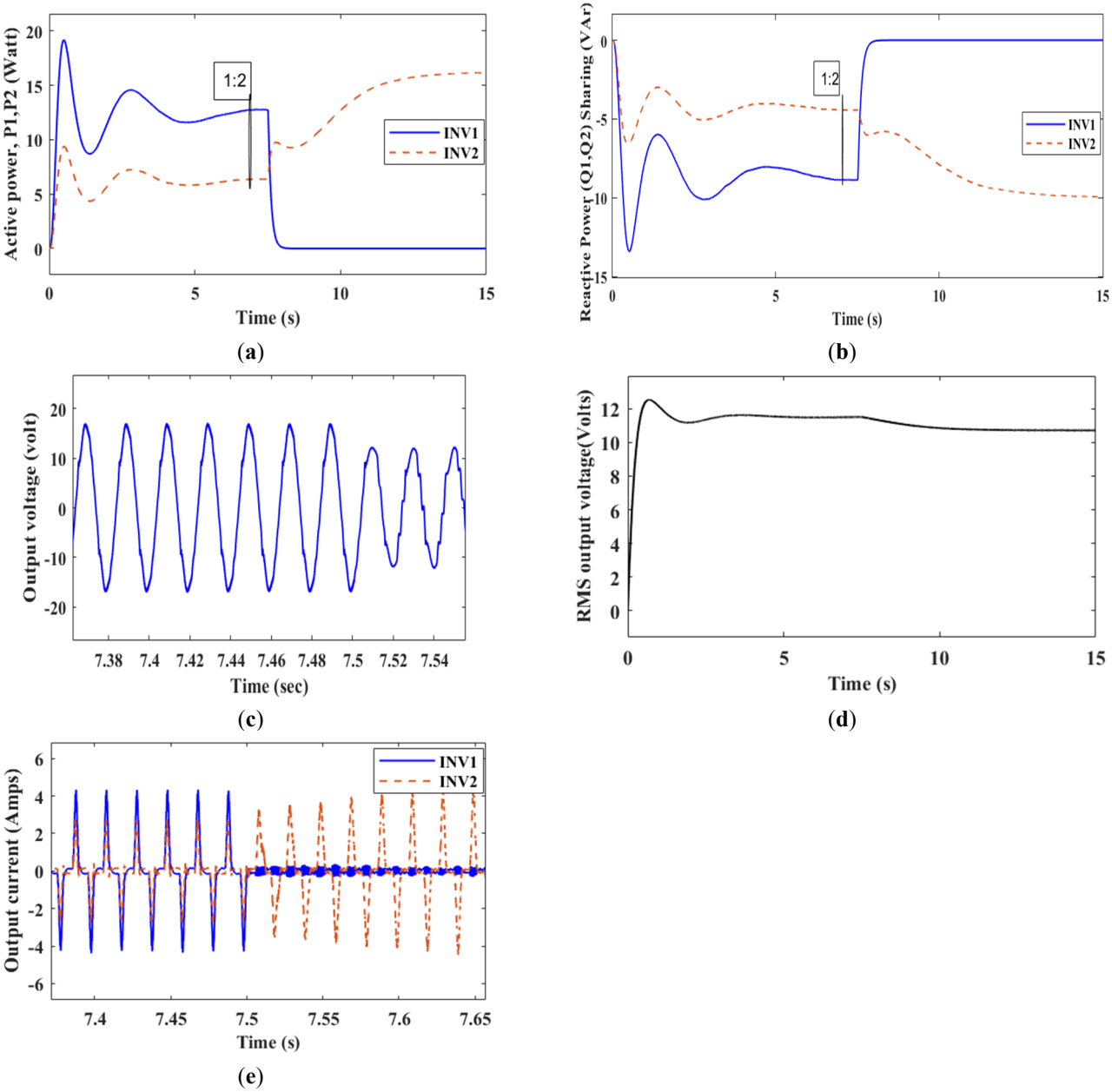

**Figure 24.** (**a**) Active power sharing *vs*. time; (**b**) Reactive power sharing *vs*. time; (**c**) RMS output voltage; (**d**,**e**) output voltage *vs*. time; (**f**) Output current *vs*. time and (**g**) inductor current *vs*. time.

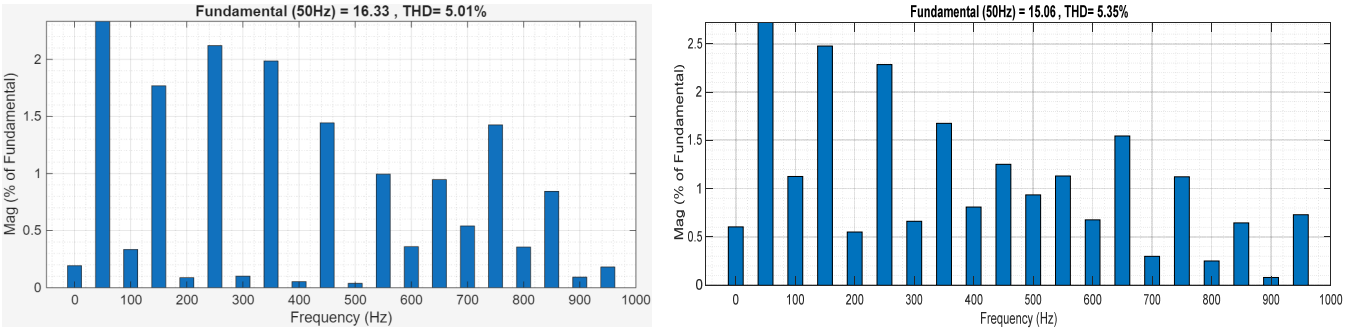
### *7.4. Simulation Results with BHC and Modified BHC Strategy*

The BHC strategy is applied to reduce $THD_v$ in case of nonlinear load-1, connected to two parallel operating inverters. Further, the modified BHC approach is tested for nonlinear load-2 (single phase rectifier followed by regulated buck converter), shown in Figure 20b, to prove its effectiveness.

#### 7.4.1. Simulation Results with Nonlinear Load-1

A system of two single phase resistive inverters operating in parallel is simulated for 15 s to verify the design. The robust droop control structure is adopted for proportional power sharing as shown in Figure 8, in which resistive droop control equations are used. The droop coefficients are $m_{iR}$, $n_{iR}$ and $K_e$ is constant. $E^*$ and $\omega^*$ are the rated voltage and frequency of the system. Initially, inverter-1 (50 VA) and inverter-2 (25 VA) are operated in parallel to supply a nonlinear load-1, $Z_L$ (full bridge rectifier with LC filter, $L_{NL}$ = 150 µH and $C_{NL}$= 1000 µF, $R_{NL}$ = 9 Ω). At $t$ = 7.5 s, inverter-1 (50 VA) is disconnected, and load is shared by inverter-2 only. The parameters are given in the Table A1 (see Appendix A). The simulation results are shown in Figure 25.

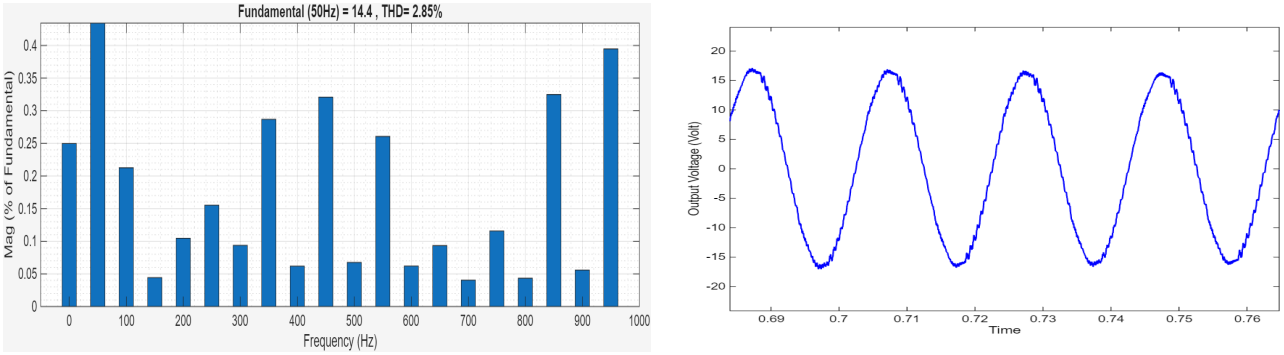





(**f**) (**g**)

**Figure 25.** (**a**) Active power *vs*. time; (**b**) Reactive power *vs*. time; (**c**) output voltage *vs*. time; (**d**) RMS output voltage *vs*. time; (**e**) output current *vs*. time; (**f**) %THD of output voltage (inverter 1, 2 operational); (**g**) %THD of Load voltage (inverter 2 operational only).

The instantaneous output voltage and $THD_v$ with further development of BHC strategy are shown in Figure 26. The quality of output voltage improves to much better extent.




(**a**) (**b**)

**Figure 26.** Modified BHC strategy. (**a**) FFT analysis of output voltage; (**b**) instantaneous output voltage.

It is important to observe from the FFT analysis that the total harmonic distortion of the output voltage with the BHC strategy is improved significantly. It is reduced to 5%, which was 15–20% in the case of capacitive inverters. Therefore, the BHC strategy with robust droop control supersedes the strategy of capacitive inverters. The active and reactive power sharing for all discussed cases has been shown in Table 7. The BHC strategy is developed further to enhance the quality of output that led $THD_v$ to 2.85%, recommended by IEEE-519 standard. The individual harmonic content in the output voltage (fundamental, $h_3$, $h_5$, …, *etc.*) has been listed in Table 8. Subsequently, Table 9 shows the comparison among four methods (BHC, modified BHC, capacitive inverter, and HDC). Among all, modified BHC outperforms in mitigating $THD_v$ in the case of highly nonlinear loads.

### 7.4.2. Simulation Results with Nonlinear Load-2

The effectiveness of modified BHC is evaluated in case of nonlinear load case-2. The active and reactive power sharing responses are illustrated in Figure 27a,b, respectively, followed by FFT analyses performed with and without the modified BHC strategy.

Note: While applying modified BHC in case of nonlinear load-2, the ratings of two inverters have been interchanged (now INV1-25 VA, INV2-50 VA). The approach effectively reduces the $THD_v$ from 19% (without equipping the strategy) to 1% (with equipping the strategy). Detailed simulation parameters are given in Table A1.

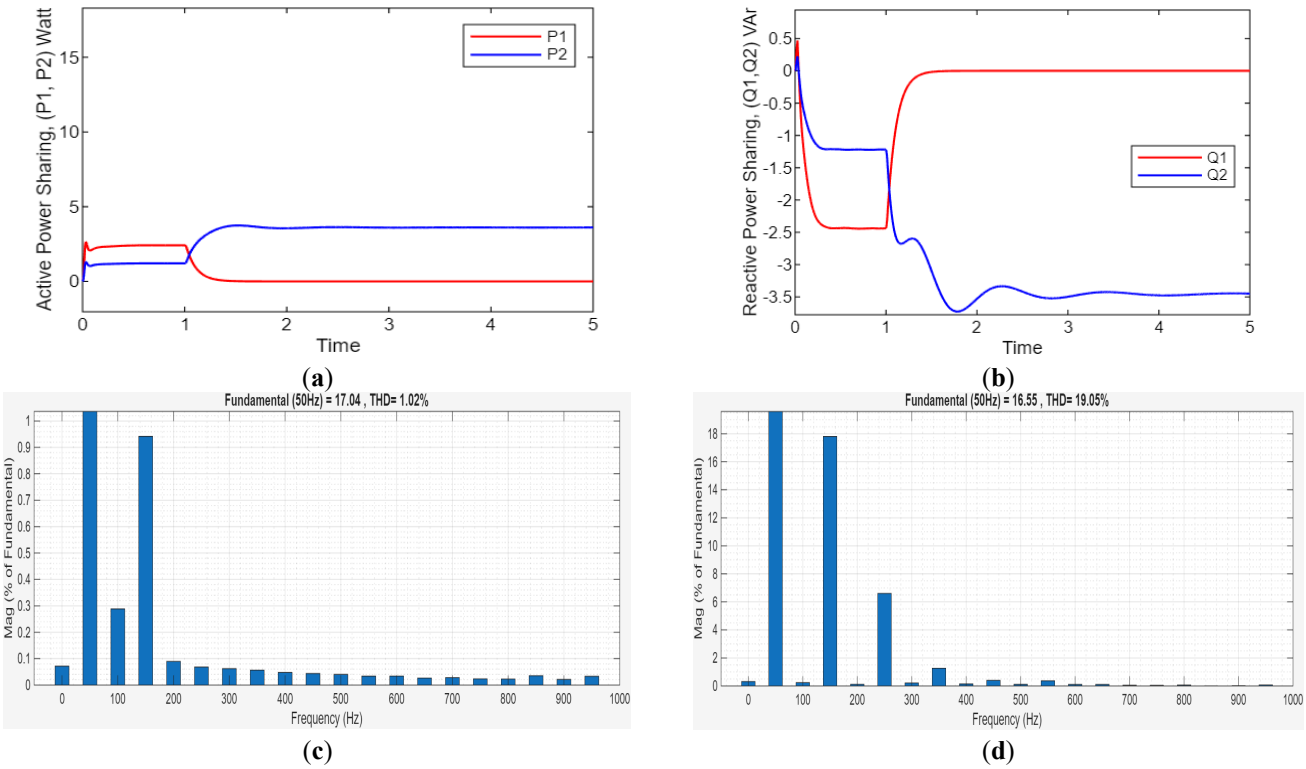



**Figure 27.** Nonlinear load-2. (**a**) Active power sharing; (**b**) reactive power sharing; (**c**) $THD_v$ (with modified strategy); (**d**) $THD_v$ (without modified strategy).

**Table 7.** Load sharing during parallel operation of inverters.

| Strategy | Parallel Operation | Active Power (Watt) | Reactive Power (Var) |
|---|---|---|---|
| C inverter (Linear Load) | 2 inverters | $P_1 = 10.53$, $P_2 = 5.26$ | $Q_1 = -1.312$, $Q_2 = -0.6567$ |
| C inverter (Nonlinear Load) | 2 inverters | $P_1 = 12.89$, $P_2 = 6.468$ | $Q_1 = -7.902$, $Q_2 = -3.954$ |
| C inverter (Nonlinear Load) | 3 inverters | $P_1 = 10.79$, $P_2 = 5.384$, $P_3 = 3.603$ | $Q_1 = -7.510$, $Q_2 = -3.745$, $Q_3 = -2.50$ |
| BHC (Nonlinear Load) | 2 inverters | $P_1 = 12.360$, $P_2 = 6.180$ | $Q_1 = -8.399$, $Q_2 = -4.199$ |

**Table 8.** Individual harmonic components relative to the fundamental.

| Frequency (Hz) | Corresponding Harmonic Component | Harmonic Content w.r.t Fundamental (%) |
|---|---|---|
| 50 | Fundamental | 100 |
| 150 | $h_3$ | 0.04 |
| 250 | $h_5$ | 0.16 |
| 350 | $h_7$ | 0.29 |
| 450 | $h_9$ | 0.32 |
| 550 | $h_{11}$ | 0.26 |
| 650 | $h_{13}$ | 0.09 |
| 750 | $h_{15}$ | 0.12 |
| 850 | $h_{17}$ | 0.32 |

**Table 9.** Comparison among strategies.

| Strategy | $THD_v$ (in %) |
|---|---|
| BHC | 5 |
| BHC with modification | |
| (i) nonlinear load-1 | 2.85 |
| (ii) nonlinear load-2 | 1.02 |
| Integral control (capacitive inverter) | 15 |
| HDC [7] | 9.4 |

## 8. Conclusions and Future Work

In this paper, an analytical approach is followed to design an integral controller parameter for 1-Φ inverter in order to achieve the objective of reduced total harmonic distortion in the output voltage. Its optimum design is ensured to reduce THD in the output voltage as well as proportional power sharing to the load. The drawbacks of conventional droop control and its remedial measures are highlighted by incorporating the robust droop control as far as parallel operation of two inverters is concerned. The replacement of an integrator by a PI controller in the PV (active power-voltage) loop is discussed to derive the new possible structure. The small signal stability analysis ensures the stable operation for a certain output impedance angle range. Subsequently, the state space matrix is formed, and eigenvalue/PF analysis is done to identify the dominant state variables. The power sharing ratio of two/three parallel operated inverters is calculated for a test example (both for linear and nonlinear loads) through time domain simulation. Further, the BHC strategy and its modified form, equipped with robust droop control is discussed to enhance the voltage quality for a nonlinear load. The time domain simulation result proves its superiority over the capacitive inverter in terms of %THD of the output voltage. Application of the controllers can be extended to grid connected and three phase inverters. Additionally, the discussion is likely to be extended experimentally by hardware-in-the-loop testing setups in the future.

## Appendix A

$$s\Delta\delta(s) = m_C \frac{\omega_f}{s+\omega_f}\left(V_o \frac{(\cos\delta\cos\theta + \sin\delta\sin\theta)}{Zo}\Delta E(s) + \frac{E\,V_o(-\sin\delta\cos\theta + \cos\delta\sin\theta)}{Zo}\Delta\delta(s)\right) \quad (A1)$$

$$s\Delta E(s) = \frac{\omega_f}{s+\omega_f}(n_C \Delta Q(s)) \quad (A2)$$

A polynomial in ‘s’ is formed by substituting ΔE(s) in Equation (A1). ‘s’ is laplace operator.

$$As^4 + Bs^3 + Cs^2 + Ds + E = 0 \quad (A3)$$

where A, B, C, D and E are functions of inverter output impedance angle.

**Table A1.** Detail parameters for resistive inverter (BHC).

| Parameters | Value | Unit |
|---|---|---|
| $K_e$ | 10 | |
| $m_{1R}$ | 0.1 | rad/Var |
| $m_{2R}$ | 0.2 | rad/Var |
| $n_{1R}$ | 0.4 | V/Watt |
| $n_{2R}$ | 0.8 | V/Watt |
| $K_1$ (virtual resistor) | 2 | |
| $K_2$ (virtual resistor) | 4 | |
| $\xi$ | 0.01 | |
| $K_9$ ($h = 9$) | 1 | |
| $K_7$ ($h = 7$) | 2.5 | |
| $K_5$ ($h = 5$) | 10 | |
| $K_3$ ($h = 3$) | 14 | |
| $r_{esr}$ | 1 Ω | |

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## Author Contributions

The details of the individual and collective contributions are presented as follows: Conceptualization, S.B.; Methodology, S.B.; Software, S.B.; Writing—Original Draft Preparation, S.B.; Writing—Review & Editing, V.S. and M.K.; Supervision, V.S. and M.K.; Funding Acquisition, Not Applicable.

## Ethics Statement

Not applicable.

## Informed Consent Statement

Not applicable.

## Data Availability Statement

The data, supporting the findings of this study are available from the corresponding author upon reasonable request.

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## Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## Glossary

| | |
|---|---|
| $C$ | filter capacitor of H bridge inverter (μF) |
| $C_o$ | Virtual capacitor or coefficient of integral controller (μF) |
| $E^*$ | reference voltage in voltage–reactive power droop control (Volts) |
| $f_s$ | switching frequency in Hz |
| $F$ | frequency of system in Hz |
| $i/i_L$ | current in filter inductance (in Amps) |
| $h$ | harmonic number |
| HDC | harmonic droop control |
| $K_e$ | constant used in robust droop control scheme/structure |
| $K_1$ | virtual resistance (unit in ohms) used in robust droop control of resistive inverter1 |
| $K_2$ | virtual resistance (unit in ohms) used in robust droop control of resistive inverter2 |
| $K_h$ | $h$-th harmonic coefficient in the transfer function of $K_r$ |
| L | filter inductance of H bridge inverter (mH) |
| $L_{NL}$, $C_{NL}$, $R_{NL}$ | nonlinear load parameters |
| $m_{ic}$ | frequency–active power droop coefficient of capacitive inverter (rad/Watt) |
| $m_{iR}$ | frequency–reactive power droop coefficient of resistive inverter (rad/Var) |
| $n_{ic}$ | voltage–reactive power droop coefficient of capacitive inverter (Volt/Var) |
| $n_{iR}$ | voltage–active power droop coefficient of resistive inverter (Volt/Watt) |
| P | active power (Watt) |
| Q | reactive power (Var) |
| RDC | Robust droop control |
| $S_i$ | rating of inverters in VA |
| $V_{DC}$ | input DC voltage to H bridge inverter |
| $v_o$ | load voltage (volts) |

| | |
|---|---|
| $\omega^*$ | reference frequency (rad/sec) in (i) frequency–active power droop characteristics of capacitive inverter and (ii) frequency–reactive power droop characteristics of resistive inverter |
| $Z_o$ | Inverter output impedance (in ohms) |
| $Z_L$ | Load impedance (in ohms) |
| $\xi$ | damping factor in the transfer function of $K_r$ |
| $THD_v$ | voltage THD |

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