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Optimal Control and Configuration of Hybrid Parallel Si/SiC Switch-Based ANPC Converter for Off-Board EV Chargers

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ABSTRACT: This paper presents an optimal switching strategy and a cost-effective hybrid configuration employing silicon (Si) IGBTs and silicon carbide (SiC) MOSFETs in a three-level active-neutral-point-clamped (ANPC) converter for high-power off-board electric vehicle (EV) chargers. A three-stage switching scheme is proposed to achieve balanced current sharing and minimize switching losses over a wide load range. In addition, a cost-saving function (CSF) is introduced to quantify the total lifecycle cost of the converter utilizing hybrid parallel switch sets, encompassing both the initial device procurement cost and the operating cost arising from power losses over the system lifetime. The proposed CSF effectively identifies the optimal hybrid switch configuration for the ANPC converter. PLECS simulations using actual device data and characteristics from multiple suppliers demonstrate that the proposed design achieves up to a 12.02% reduction in power losses compared with single-Si-switch designs and a 66.42% cost saving relative to all-wide-bandgap solutions, thereby providing an effective efficiency–cost trade-off for next-generation EV charging systems.

Keywords: ANPC; Parallel switches; Three-stage switching technique; Hybrid structure; Loss analysis

1. Introduction

Electric vehicles (EVs) have emerged as a key solution for decarbonizing road transportation and have been rapidly deployed worldwide in recent years. In addition to reducing greenhouse gas emissions, EVs can also improve energy efficiency and reduce maintenance requirements. A key challenge for EV adoption, however, lies in the charging infrastructure. Although technological breakthroughs have dramatically reduced charging times and extended driving ranges, with ultra-fast charging now approaching refueling speeds and average ranges exceeding 300 miles, consumer perception of these issues remains a key barrier. Range anxiety and charging time continue to rank among the top concerns for potential buyers in major markets, pointing to a persistent gap between technological progress and public confidence. To match the refueling experience of internal combustion engine (ICE) vehicles, fast chargers with power ratings up to 400 kW and dc-link voltages above 800 V are required [1–3]. Multilevel converters are widely adopted in such high-power applications due to their reduced device voltage stress, improved efficiency, lower total harmonic distortion (THD), and electromagnetic interference (EMI) [4,5]. The active-neutral-point-clamped

(ANPC) converter is among the most suitable inverter topologies, as it enables bidirectional operation for both G2V and V2G modes. Compared with the conventional NPC converter, the ANPC offers advantages such as more available switching states, reduced switching stress, and enhanced fault-tolerant capability.

However, the realization of megawatt-level off-board chargers demands improved current-handling capability. One common solution is to use power switching devices connected in parallel. Although this approach can alleviate high current stress on individual devices, it may suffer from uneven current sharing and dynamic-response mismatch between devices, which can lead to high thermal stress and eventual system failures. Recent technological developments in wide-bandgap (WBG) semiconductors have facilitated the adoption of advanced switching devices, including silicon carbide (SiC) and gallium nitride (GaN)-based MOSFETs. Compared with their silicon (Si) counterparts, they have high voltage blocking capability, high switching frequency, and can withstand excessive thermal stress [6–8]. The integration of these advanced semiconductor devices into EV chargers is expected to improve energy conversion efficiency, reduce circuit size, and enhance robustness. However, completely replacing Si IGBTs with SiC MOSFETs is not yet practical because the current ratings of commercially available SiC MOSFETs are generally lower than those of Si IGBTs, while SiC devices remain significantly more expensive than Si devices.

To take full advantage of the complementary characteristics of the two device types, hybrid parallel switch configurations that pair a relatively low-current SiC MOSFET with a higher-current Si IGBT have been proposed. Song et al. employed a hybrid topology in high-voltage systems and achieved reduced turn-off losses by commutating the current from the IGBT to the MOSFET prior to turn-off, with a controlled delay applied to the MOSFET's switching signal [9]. However, the IGBT turn-on loss was not properly considered in their study, and the hybrid structure's performance was not validated within a specific inverter topology. Elsewhere, alternative switching strategies have been explored, including a three-stage load-current-dependent sharing scheme proposed for paralleled low-current SiC MOSFET and high-current Si IGBT pairs.

However, as shown in [10], during the high-current stage, by turning the IGBT on first and off last, the device bears the high di/dt and inrush current, so its switching loss is scarcely reduced. Furthermore, current commutation between the IGBT and MOSFET branches induces large di/dt, exciting parasitic components and causing ringing, overshoot, and EMI. The commutation-driven di/dt, together with bus/package inductance, also yields over-voltage spikes and dynamic-avalanche risk, which is aggravated in ANPC, especially at neutral-point clamping switches, raising the likelihood of midpoint-voltage imbalance. Furthermore, Woldegiorgis et al. utilized a paralleled hybrid device configuration in an ANPC converter, incorporating a "MOSFET-first-on, last-off" switching scheme to mitigate IGBT switching losses at low currents. However, that work did not adequately address current sharing between the two parallel switches, nor did it include a cost analysis [11].

While the hybrid configuration offers the high overcurrent capability of IGBTs and the fast, low-loss switching of SiC devices, several technical challenges remain, including: (i) control over a wide load range; (ii) transient current imbalance and parasitic mismatch; and (iii) optimization of the configuration for both efficiency and cost. Given that cost-optimal design remains largely unexplored, this paper investigates hybrid parallel switch sets for off-board fast EV chargers to address these gaps. The main contributions of this paper are summarized as follows:

- A mixed configuration combining single switches and parallel hybrid Si IGBT/SiC MOSFET switch sets is designed and analyzed to achieve an optimal trade-off between efficiency and cost for an ANPC-based off-board EV charging system.
- A flexible three-stage switching strategy is proposed for full-load-range operation of the ANPC converter, effectively leveraging the high-speed, low-loss switching characteristics of SiC devices and the high current-handling capability of Si IGBTs.

- A cost-saving function (CSF) is proposed for the first time to quantify the total lifecycle cost of a converter employing hybrid parallel switch sets. It accounts for both the initial procurement cost and the operating cost associated with power losses over device lifetime. It is demonstrated to be effective in identifying optimal single-switch and hybrid-parallel switch-set configurations for an ANPC circuit with respect to the loss–cost trade-off.

The remainder of the paper is organized as follows: Section 2 presents the ANPC converter-based EV charger and the parallel hybrid switch architecture. Section 3 analyzes parallel switch control strategies and proposes the three-stage switching scheme. The loss analysis of switch sets is presented in Section 4. Section 5 introduces the cost-efficiency optimization function and the proposed hybrid configuration. Section 6 concludes the paper.

2. Configuration of an ANPC-Based EV Off-Board Charging System with Parallel Hybrid Switches

2.1. System Configuration

The configuration of an off-board EV charger, as illustrated in Figure 1, consists of a grid-tied three-phase ANPC converter equipped with an LCL filter, while the EV battery packs are connected to the DC bus through their respective DC/DC converters.

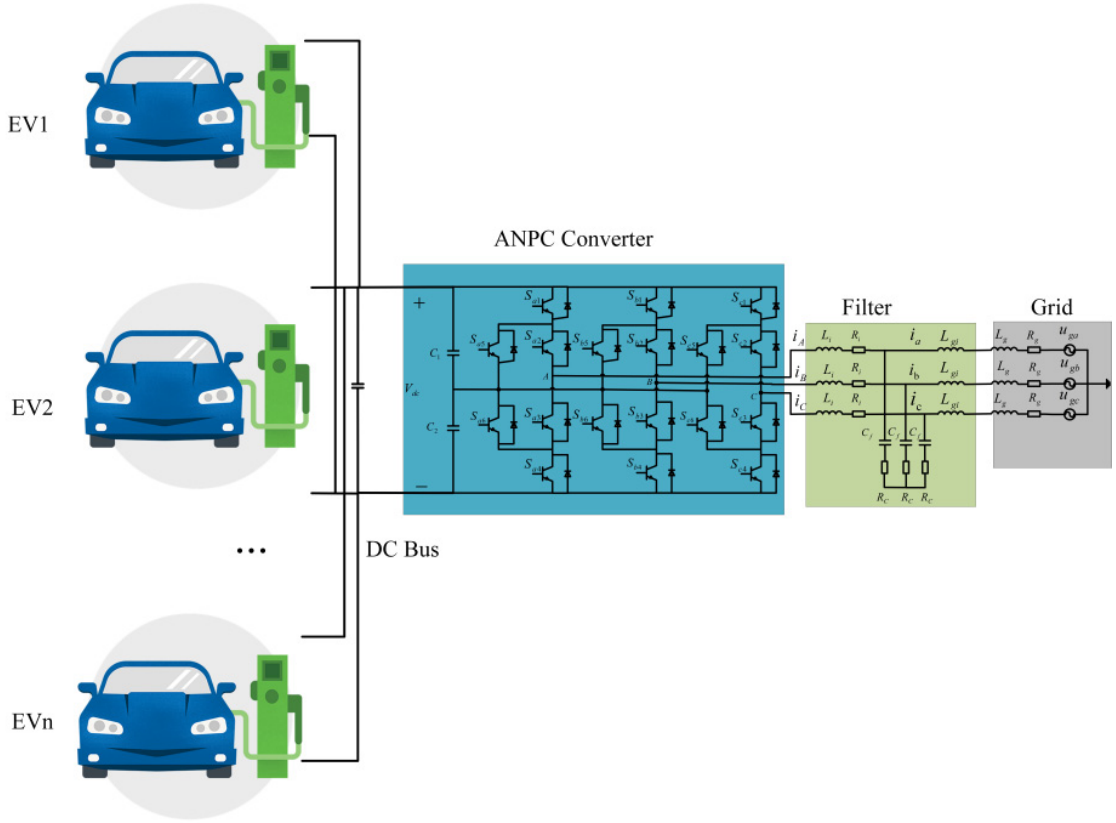


Figure 1. ANPC-based off-board EV battery charging system.

This work focuses on the AC/DC stage of the system, the grid-connected front-end rectifier/inverter that interfaces with the utility grid and provides a regulated DC bus. In this stage, the ANPC converter enables bidirectional operation for both G2V and V2G modes. Compared with the conventional NPC converter, the ANPC offers advantages such as a greater number of available switching states, reduced switching stress, and enhanced fault-tolerant capability. Each of its three-phase legs consists of six controllable switch-diode pairs. Taking phase A as an example, two series-connected switches (S_{a1} and S_{a2})

are tied to the positive DC bus; another pair (S_{a3} and S_{a4}), to the negative DC bus; while S_{a5} and S_{a6} are linked to the neutral point formed by the two DC-link capacitors.

2.2. Parallel Hybrid Switches

During peak periods of rapid charging multiple EV batteries, charging stations may face high current demands. A practical way to reduce power losses and extend device lifespan in this scenario is to operate multiple devices in parallel using the same gate signal, thereby alleviating electrical and thermal stress on each switch. However, the current imbalance may arise from layout asymmetry, gate-drive inconsistencies, and device parameter variations, leading to some devices being overstressed. Unlike directly paralleling identical devices, a hybrid switch set combines the low switching losses of SiC MOSFETs, attributed to their wide-bandgap properties, with the low cost and high overload capability of Si IGBTs. Taking a two-device parallel switch topology as an example, Figure 2 illustrates an ANPC bridge employing a hybrid switch configuration.

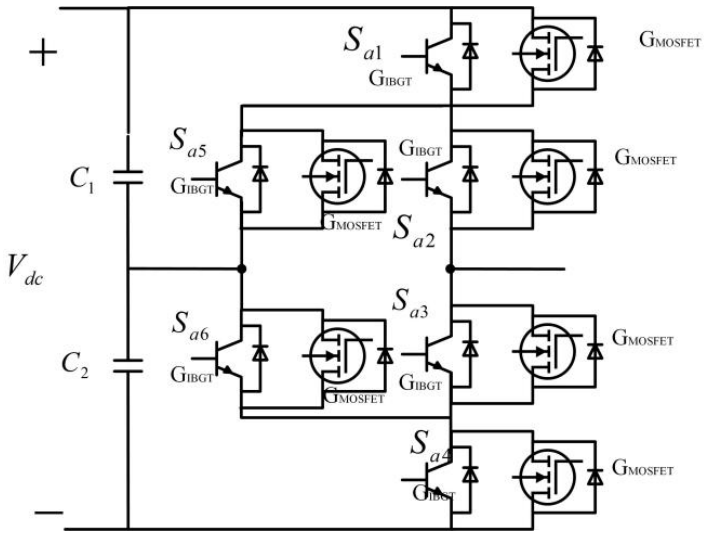


Figure 2. Phase leg circuit of an ANPC using hybrid parallel switch-sets.

Typically, each hybrid switch set consists of a high-current-rated Si IGBT paired with a lower-current-rated SiC MOSFET. This configuration reduces electrical stress on individual devices and achieves higher efficiency than conventional parallel configurations.

3. Control Strategies of Parallel Hybrid Switches in ANPC Converter

In a parallel hybrid switch set, the on-state current should ideally be shared between the two devices in proportion to their respective current ratings and on-state resistances. In practice, however, this ideal distribution is difficult to achieve due to differences in device physics and asymmetric circuit parasitics between the Si IGBT and the SiC MOSFET, which may lead to momentary overcurrent in the MOSFET. It is therefore essential to devise switching strategies that account for the distinct physical characteristics of each device, so as to ensure proper load current sharing, minimize losses, and guarantee safe operation.

3.1. Switching Modes of Parallel Hybrid Switches

Four switching modes for parallel switch sets have been proposed, as illustrated in Figure 3 [12,13], where S_{SiC} denotes the gate signal for the SiC MOSFET and S_{IGBT} is the one for the Si IGBT. For Mode 1, shown in Figure 3a, identical gate signals are applied to both switches, enabling current sharing during the switching cycle. However, it does not fully utilize the fast switching capability of the SiC MOSFET, and

the tail current of the Si IGBT during turn-off will cause significant switching losses. In Mode 2, the IGBT is turned on first and turned off last. This strategy accounts for parasitic inductance differences during the turn-on period, but it still leads to higher switching losses due to the IGBT's tail current. In Mode 4, the IGBT is turned on first, and the MOSFET is closed later. This is intended to mitigate inadvertent IGBT turn-on triggered by the high dv/dt that happens during the MOSFET's turn-off transient, but it may result in high turn-on losses of the IGBT.

Mode 3 is considered the most effective strategy to fully exploit the complementary characteristics of both devices. Figure 4 illustrates the voltage and current waveforms in this mode, where V_H is the voltage across the hybrid switch set, I_{SiC} and I_{IGBT} are the currents through the MOSFET and IGBT, respectively. In this mode, the IGBT switches on after the MOSFET with a delay of t_1. During the turn-off process, the SiC is switched off after a delay of t_2 in relation to the IGBT turn-off time. The IGBT achieves zero-voltage switching (ZVS), while the SiC MOSFET absorbs most of the switching loss, thereby eliminating IGBT tail-current loss. During the on-state period, the MOSFET conducts a smaller fraction of the load current, so the high-current-rated IGBT dominates conduction losses. However, Mode 3 may not be desirable under certain operating conditions. For instance, during periods t_1 and t_2, the SiC MOSFET is the sole active device, carrying the entire load current, which could subject it to excessive current stress, especially during peak charging periods. Furthermore, differences in device parasitic inductances may delay current transfer from the SiC MOSFET to the Si IGBT during the transient period when the IGBT is turned on. These considerations motivate the design of a switching strategy that is better suited to a wider load range.

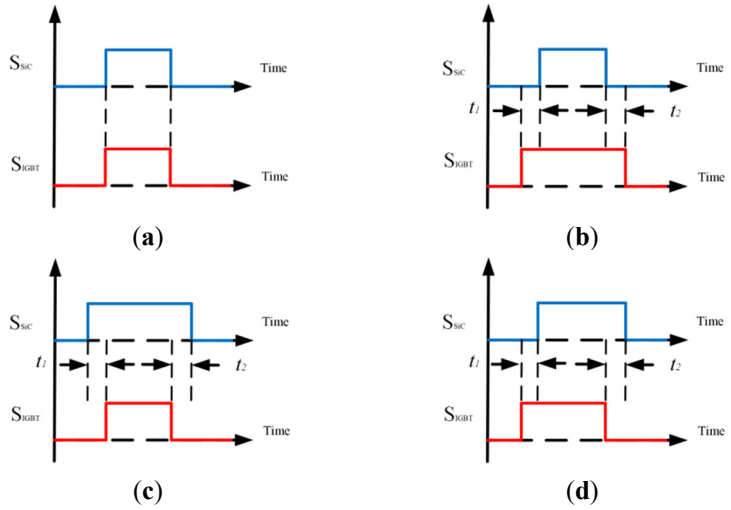


Figure 3. Switching modes for parallel switches. (**a**) Mode 1. (**b**) Mode 2. (**c**) Mode 3. (**d**) Mode 4.

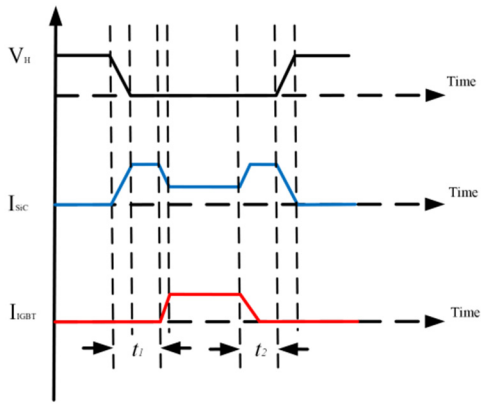


Figure 4. Device current and voltage waveforms during switching on/off transients for mode 3.

3.2. Three-Stage-Switching Control Strategy for Parallel Hybrid Switch Sets

Given that the charger operates across a full range of load conditions, a three-stage switching scheme is proposed for the ANPC's hybrid switches, with the operating stage determined by the load current magnitude. In Stage 1, when the load current falls below the boundary current I_1 (the blue region in Figure 5), the SiC MOSFET is switched on alone to conduct the load current, while the IGBT remains off. As illustrated in Figure 6 [14,15], I_1 is defined as the intersection point of the threshold voltages on the I–V curves of the specific MOSFET and IGBT; this value is approximately 20 A for the devices considered, though it may vary for other device combinations. When the output current exceeds I_1 but remains below I_2 (red region in Figure 5), Stage 2 is activated, in which both the IGBT and MOSFET operate together to share the load current under Mode 3. Stage 3 is triggered when the output current exceeds I_2, which corresponds to the Safe Operating Area (SOA) current limit of the selected SiC MOSFET. In this stage, the IGBT operates independently.

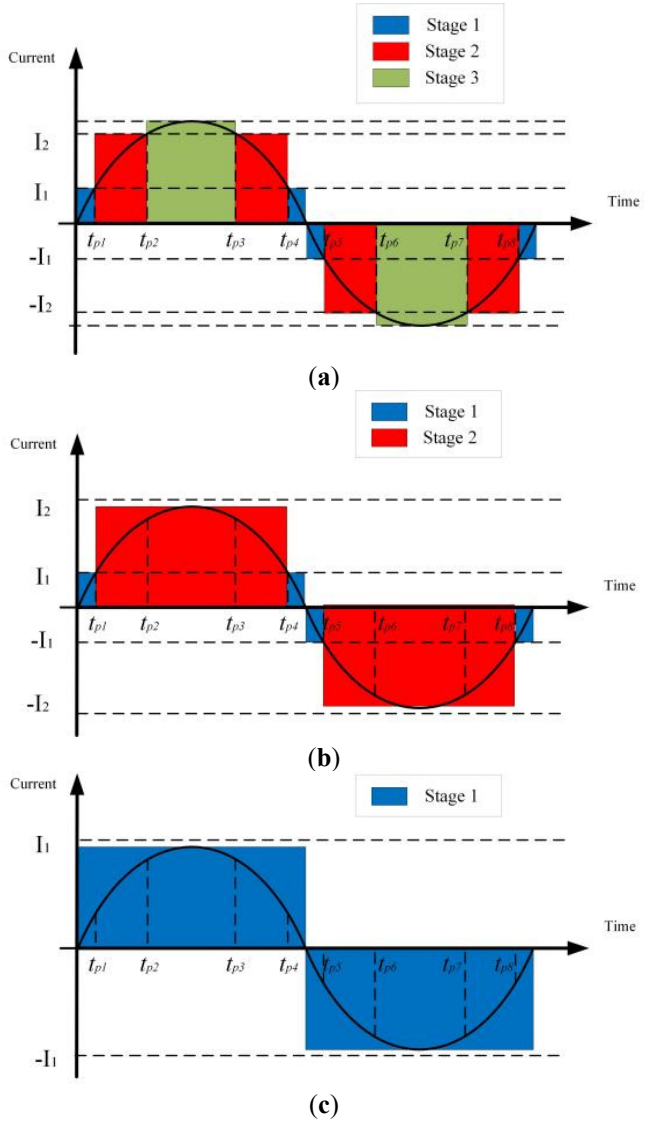


Figure 5. Three-stage switching scheme. (**a**) Three-stage mode with heavy load. (**b**) Two-stage mode with medium load. (**c**) Single-stage mode with light load.

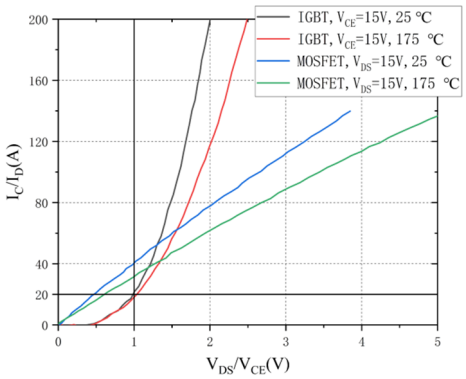


Figure 6. Typical output I–V characteristic of devices.

3.3. Loss Analysis of Hybrid Si IGBT/SiC MOSFET Switches in Parallel

The losses of the IGBT, MOSFET, and hybrid switch sets are analyzed when they are working in Stage 2. For Si IGBT, the threshold voltage $V_{The}(T_j)$ and on-state resistance $R_{CE}(T_j)$ are influenced by the junction temperature T_j of the switch [16,17]:

$$V_{The}(T_j) = V_{The\_25°C} + K_v(T_j - 25°C) \tag{1}$$

$$R_{CE}(T_j) = R_{CE\_25°C} + K_R(T_j - 25°C) \tag{2}$$

where $V_{The\_25°C}$ and $R_{CE\_25°C}$ are the threshold voltage and on-state resistance of IGBT at 25 °C, respectively; K_v, K_R are the temperature coefficients of $V_{The}(T_j)$ and $R_{CE}(T_j)$, respectively. Then, the voltage between collector and emitter $V_{CE}(t,T_j)$ can be expressed as:

$$V_{CE}(t,T_j) = V_{The}(T_j) + R_{CE}(T_j)\ \ i_{IGBT}(t,T_c) \tag{3}$$

where $i_{IGBT}(t,T_c)$ is the collector current of the IGBT and T_c is the case temperature of the power device.

Consequently, the conduction loss of the IGBT in one cycle is given as follows:

$$\begin{aligned} P_{IGBT\_Con} &= V_{CE}(t,T_j)\ \ i_{IGBT}(t,T_c)D_{IGBT}(t) \\ &= \left(V_{The\_25°C} + K_v(T_j - 25°C)\right) \times D_{IGBT}(t) \times i_{IGBT}(t,T_c) \\ &+ \left(R_{CE\_25°C} + K_R(T_j - 25°C)\right) \times D_{IGBT}(t) \times i^2_{IGBT}(t,T_c) \end{aligned} \tag{4}$$

where $D_{IGBT}(t)$ is the duty cycle of the IGBT. Another contributor to power loss is the switching loss arising from the semiconductor's intrinsic switching delays. The turn-on loss P_{IGBT_Son} and turn-off loss P_{IGBT_Soff} can also be evaluated as:

$$P_{IGBT\_Son} = f_s K_{RGon} K_{T_{j\_IGBT}} E_{IGBTon}(i_{IGBT},T_j)\left(\frac{V_{DC}}{V_N}\right)\left(\frac{I_{IGBT}}{I_{IGBT_{nom}}}\right) \tag{5}$$

$$P_{IGBT\_Soff} = f_s K_{RGoff} K_{T_{j\_IGBT}} E_{IGBToff}(i_{IGBT},T_j)\left(\frac{V_{DC}}{V_N}\right)\left(\frac{i_{IGBT}}{I_{IGBTnom}}\right) \tag{6}$$

where f_s is the switching frequency; K_{RGon} and K_{RGoff} are the influence coefficients of external gate resistance on turn-on and turn-off losses, respectively; K_{Tj_IGBT} is the temperature coefficient of losses, these parameters are highly dependent on the chip size, and all of them are set to unity for simplicity; E_{IGBTon} and $E_{IGBToff}$ are the IGBT turn-on loss and turn-off loss at nominal voltage V_N and current $I_{IGBTnom}$, respectively. Collector current i_{IGBT}, and dc voltage V_{DC}, also influence the switching losses.

The conduction loss for MOSFET can also be computed based on the fixed on-state resistance characteristic:

$$P_{MOS\_Con} = K_{Rds} i^2_{MOS}(t,T_j) R_{ds}(V_{gs},T_j) D_{MOS}(t) \tag{7}$$

where K_{Rds} is the correction coefficient of on-state resistance R_{ds}; i_{MOS} is the drain-source current of MOSFET; V_{gs} is the voltage between gate and source electrodes; $D_{MOS}(t)$ is the duty ratio of the MOSFET.

The MOSFET switching losses, including turn-on and turn-off losses, can be expressed as follows:

$$P_{MOS\_Son} = f_s K_{RGon} K_{T_{j\_MOS}} E_{MOSon}(i_{MOS}, T_j)\left(\frac{V_{DD}}{V_{DD\_nom}}\right)\left(\frac{i_{MOS}}{I_{MOSnom}}\right) \tag{8}$$

$$P_{MOS\_Soff} = f_s K_{RGoff} K_{T_{j\_MOS}} E_{MOSoff}(i_{MOS}, T_j)\left(\frac{V_{DD}}{V_{DD\_nom}}\right)\left(\frac{i_{MOS}}{I_{MOSnom}}\right) \tag{9}$$

where K_{Tj_MOS} is the temperature coefficient of losses, which can be set to unity together with gate resistance coefficients [18]; V_{DD} and i_{MOS} are the drain-source voltage and current, respectively; V_{DD_nom} and I_{MOSnom} are the test voltage and current for turn-on loss $E_{MOSon}(i_{MOS}, T_j)$ and turn-off loss $E_{MOSoff}(i_{MOS}, T_j)$. It is possible to evaluate the switching losses for a parallel hybrid switch set as:

$$E_{on} = E_{MOS\_on} + E_{IGBT\_on} + E_{C\_on} = \int_{t_{start}}^{t_{on1}} P_{MOS\_Son}dt + \int_{t_{on2}}^{t_{stable1}} P_{IGBT\_Son}dt + \int_{t_{on1}}^{t_{stable1}} (P_{MOS\_Con})dt \tag{10}$$

where E_{MOS_on} and E_{IGBT_on} are the turn-on losses for MOSFET and IGBT during intervals t_{start}–t_{on1} and t_{on2}–$t_{stable1}$, respectively, as shown in Figure 7a. E_{C_on} is the additional conduction loss of the MOSFET from t_{on1} to t_{stable}. It is evident that the IGBT switches on at a zero-voltage state, so E_{on} can be rewritten as:

$$E_{on} = E_{MOS\_on} + E_{IGBT\_on} + E_{C\_on} = \int_{t_{start}}^{t_{on1}} P_{MOS\_Son}dt + \int_{t_{on1}}^{t_{stable1}} (P_{MOS\_Con})dt \tag{11}$$

$$E_{off} = E_{MOS\_off} + E_{IGBT\_off} + E_{C\_off} = \int_{t_{off2}}^{t_{end}} P_{MOS\_Soff}dt + \int_{t_{stable2}}^{t_{off1}} P_{IGBT\_Soff}dt + \int_{t_{stable2}}^{t_{end}} (P_{MOS\_Con})dt \tag{12}$$

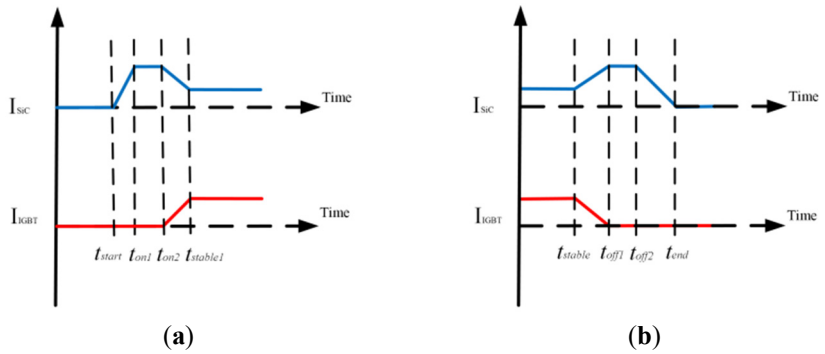
where E_{MOS_off} and E_{IGBT_off} are the turn-off losses for MOSFET and IGBT during periods t_{off2}–t_{end} and $t_{stable2}$–t_{off1}, respectively, which is shown in Figure 7b. E_{C_off} is the additional conduction loss of the MOSFET from t_{stable} to t_{off2}, and the turn-off loss of the IGBT is still approximately zero. Therefore, Equation (12) can be simplified as:

$$E_{off} = E_{MOS\_off} + E_{IGBT\_off} + E_{C\_off} = \int_{t_{off2}}^{t_{end}} P_{MOS\_Soff}dt + \int_{t_{off1}}^{t_{end}} (P_{MOS\_Con} + P_{IGBT\_Con})dt \tag{13}$$

Finally, the conduction loss of the parallel switch set during time $t_{stable1}$ to t_{stable} is given as:

$$E_{Con} = E_{MOS\_Con} + E_{IGBT\_Con} = \int_{t_{stable1}}^{t_{stable2}} P_{MOS\_Con}dt + \int_{t_{stable1}}^{t_{stable2}} P_{IGBT\_Con}dt \tag{14}$$

where E_{MOS_Con} and E_{IGBT_Con} are conduction losses during the interval from $t_{stable1}$ to $t_{stable2}$ of MOSFET and IGBT, respectively.



(**a**) (**b**)

Figure 7. The switching process of hybrid switches. (**a**) Turn-on process of the hybrid switch. (**b**) Turn-off process of the hybrid switch.

In summary, the switching losses are mainly generated by the SiC MOSFET, as given in Equations (11) and (13), whereas the losses due to the IGBT tail current are avoided. The loss analysis for stages 1 and 3 is similar to that for a single-switch application.

3.4. PWM Scheme of ANPC-Based Converters

The power losses of ANPC converters using only Si IGBTs under different PWM schemes were investigated in [19]. The results show that PD-PWM yields the lowest power loss among the compared PWM schemes and has strong potential for hybrid switch structures. The ANPC topology using the PD-PWM scheme provides four switching states as listed in Table 1, including one positive state and one negative voltage state, as well as two zero-voltage states (ZVS). The PD-PWM utilizes two carrier waves of the same magnitude and frequency, which are level-shifted in the positive and negative sinusoidal voltage regions. Figure 8a–c display the positive and negative current flow paths and two ZVSs. The switches can also be grouped according to their switching frequencies, as shown in Figure 8d. Switches S_{a2} and S_{a3} are assigned to the high-switching-frequency group and are therefore responsible for most of the switching losses. The remaining switches are either kept closed or open for half of the reference signal cycle and consequently contribute primarily to conduction losses. The control signals for all switches are shown in Figure 9a–f.

Table 1. Switching states of the ANPC converter.

States	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}
Positive	on	on	off	off	off	on
0_+	on	off	on	off	off	on
0_-	off	on	off	on	on	off
Negative	off	off	on	on	on	off

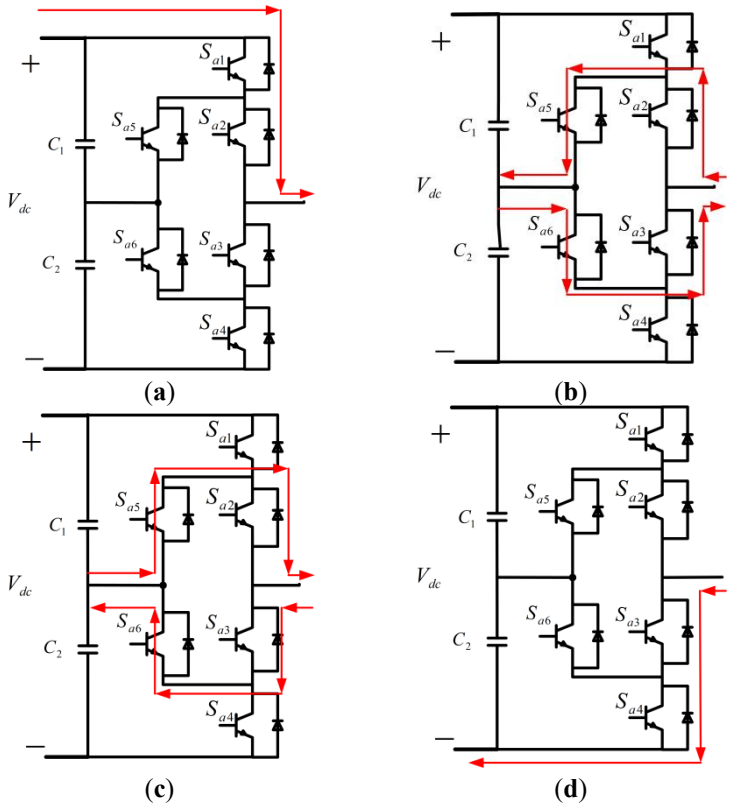


Figure 8. Current conduction directions under PD-PWM control. (**a**) Positive current flow. (**b**) Positive and negative zero-voltage states. (**c**) Negative current flow. (**d**) Complementary switch groups.

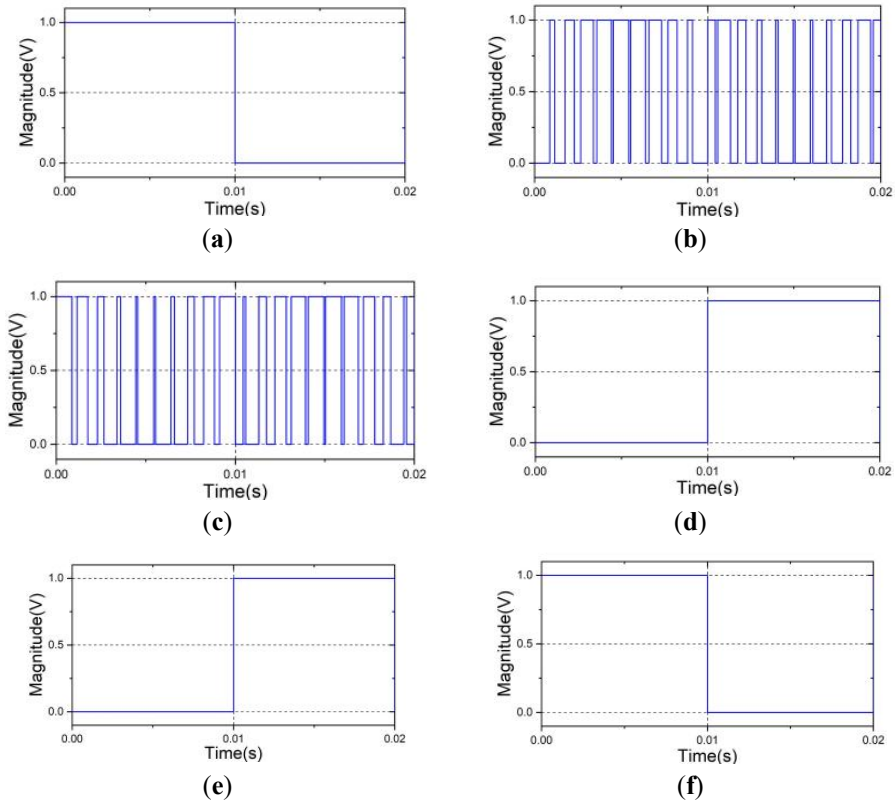


Figure 9. Switching signals for 6 switches using PD-PWM. (**a**) S_{a1}. (**b**) S_{a2}. (**c**) S_{a3}. (**d**) S_{a4}. (**e**) S_{a5}. (**f**) S_{a6}.

4. Loss Evaluation of ANPC with Parallel Hybrid Switch Set

4.1. Controller Architecture and Device Selection

To quantitatively evaluate the losses of an ANPC converter employing hybrid switch sets for an off-board EV charging system, a case study is conducted in PLECS on a 40 kW, 800 V system. The case study adopts a two-switch hybrid topology, although the methodology is readily extensible to higher power levels by increasing the number of parallel switches. The system controller architecture is illustrated in Figure 10, where the measured three-phase voltages and currents are mapped to the *αβ* and *dq* frames, respectively, using the PLL-generated phase angle *ωt*. System parameters are summarized in Table 2.

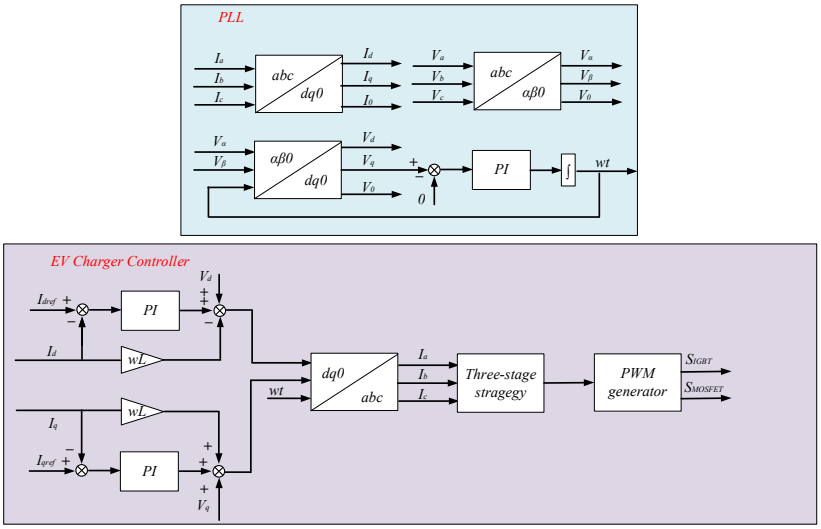


Figure 10. Block diagram of the system controller.

By setting the *d*-axis reference current I_{dref}, the system's charging/discharging power can be regulated, while the *q*-axis reference current (I_{qref}) is fixed at zero. The variables in the *dq* frame are decoupled, and the errors between the measured and reference variables are regulated by PI controllers, then mapped back to the three-phase domain. Finally, in conjunction with the three-stage control scheme and PWM modulation, the synthesized commands generate the switching signals for the IGBT and MOSFET devices.

Table 2. Parameters of the system.

Parameters	Value	Parameters	Value
Input voltage, V_{DC}	800 V	Grid-side inductance, L_g	1.58 mH
Input capacitors, C_1, C_2	5 mF	Filter capacitors, C_f	25 μF
Filter inductance, L_i	2 mH	Grid voltage, u_{gi}	220 V
Switching frequency, f_s	10,000 Hz	Resistance of inductance, R_i	1 mΩ
Grid-side resistance, R_g	0.8929 Ω	Proportional coefficient, K_p	100
Integral coefficient, K_I	1	Turn-on delay, t_1	0.2 μs
Filter grid-side inductance, L_{gi}	60 μH	Damping resistance, R_C	0.5 Ω
Threshold current of IGBT, I_1	20 A	Maximum current of SOA, I_2	80 A
Turn-off delay, t_2	0.6 μs		

In the proposed three-stage switching scheme, the SOA current limit is a key threshold for distinguishing Stage 2 from Stage 3. In this study, several low-current-rated SiC MOSFETs from Wolfspeed with different SOA current limits are analyzed, namely: C3M0025065K (70 A, $15.58) [20], C3M0045065K (49 A, $10.3) [21], C3M0060065K (37 A, $8.96) [22] and C3M0120065K (22 A, $3.53) [23], all prices and ratings are as of the time of writing. Using the same IGBT IKQ120N60TXKASA (120 A, $14.01, as of the time of writing) and the aforementioned SiC MOSFETs with different SOA current limits, the losses of each parallel switch set using the three-stage strategy with an output current of 100 A are shown in Figure 11, and the key parameters of each device are also given in Table 3. The results clearly show that devices with higher SOA current limits achieve lower total losses, which demonstrates the efficacy of the proposed three-stage control scheme.

Table 3. Part Numbers and Key Parameter Values of Si IGBT and SiC MOSFET devices.

Devices	Rated Current (A)	SOA (A)	Price ($)	R_{CE}/R_{DS} (mΩ)	K_R	K_v
C3M0120065K [ref]	22	24	3.53	120	0.013	3.2×10^{-4}
C3M0060065K [ref]	37	40	8.96	60	0.004	1.3×10^{-4}
C3M0045065K[ref]	49	50	10.3	45	0.0026	1.1×10^{-4}
C3M0025065K [ref]	70	80	15.58	25	0.0013	5.3×10^{-5}
C3M0015065K [ref]	120	150	58.74	15	7.06×10^{-4}	3.3×10^{-5}
IKQ120N60TXKASA [ref]	120	500	14.01	16	0.0016	1.63×10^{-5}

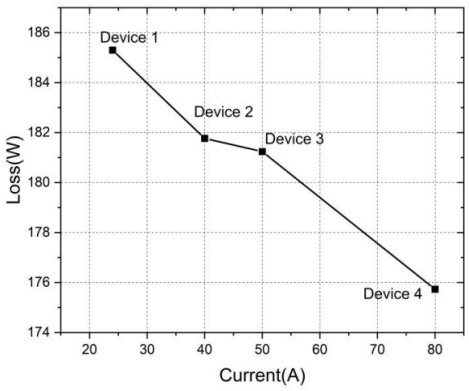
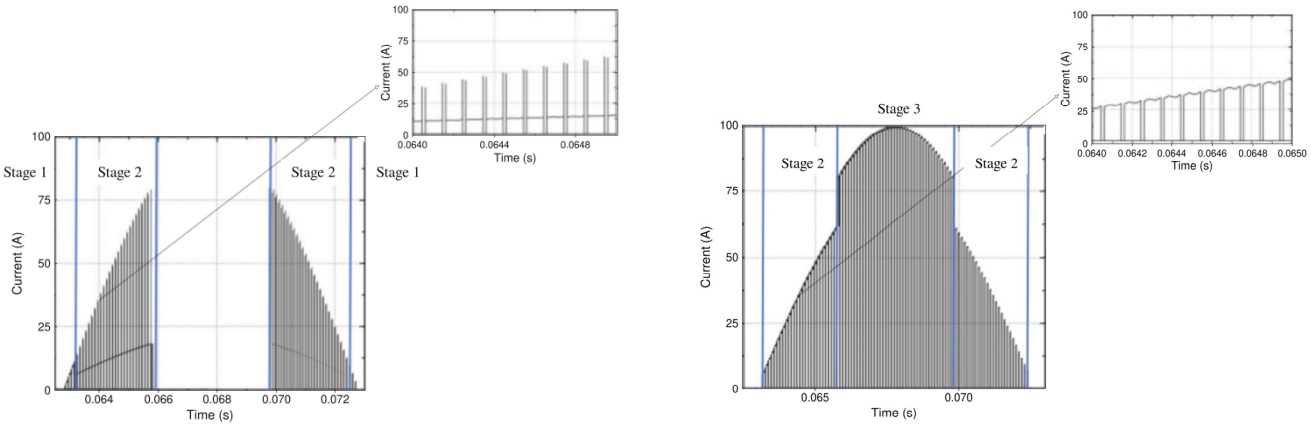


Figure 11. Losses of SiC MOSFET with different SOA limits.

As shown in Figure 5, appropriate time intervals should be applied to ensure that the SiC device is fully turned on before the Si IGBT is turned on. Likewise, the turn-off of the SiC device can only be triggered when the Si IGBT is completely switched off due to the tail current. Among all devices selected and listed in Table 3, the longest turn-on time is 76 ns, and the longest turn-off time is 343 ns. To avoid cross-conduction, the system's turn-on and turn-off delays should be set to roughly 2–3 times of the switches' turn-on and turn-off times, respectively. Accordingly, the simulation uses a turn-on delay of 0.2 µs and a turn-off delay of 0.6 µs.

However, MOSFETs with higher SOA limits are substantially more expensive; the price of a C3M0015065K (120 A) is nearly triple that of a C3M0025065K. In this study, the latter is chosen for use in the hybrid switch set, and the SOA current I_2 is set to 80 A. To implement the proposed three-stage switching scheme, the operating ranges of the two devices must be defined appropriately to leverage the advantageous SiC switching features, on-state overloading capabilities of the Si device, and lower losses and stress on individual switches. Figure 12 shows the current flowing through the two devices when the three-stage-switching scheme is applied. The selected devices for further analysis are IGBT IKQ120N60TXKASA and MOSFET C3M0025065K.



(**a**) (**b**)

Figure 12. Current is flowing through the parallel switches. (**a**) Current of SiC MOSFET at stage 1 and stage 2. (**b**) Current of Si IGBT at stage 2 and stage 3.

4.2. Loss Analysis of Parallel Switches Under the Three-Stage Scheme

Using the same topology, the proposed three-stage strategy is compared with the conventional Mode 1 scheme. Figure 13 shows the conduction and switching losses for each of the six parallel switch sets of an ANPC phase leg under PD-PWM modulation with the three-stage switching scheme applied.

In Figure 13a, the converter operates at a low current below 20 A. According to the proposed three-stage switching scheme shown in Figure 5c, only the SiC MOSFET is active; hence, the converter operates in a single-switch mode. In terms of the total loss under light load, the three-stage strategy produces a power loss of 9.1 W, which is the same as the traditional strategy using Mode 1 since only the MOSFET is active. When the ANPC converter operates at a medium load current of 50 A, both the SiC and Si devices in the parallel switch set are active. The losses for SiC and Si devices in each of the switch sets are evaluated within the three-stage switching scheme, as shown in Figure 5b; the results are illustrated in Figure 13b. The conduction loss of the SiC MOSFET is the dominant one in all six switch sets, this is due to its higher on-state resistance characteristics. Specifically, the total power loss is 143.3 W for the proposed scheme, while for the Mode 1 scheme, the loss is 147.5 W due to the losses caused by the tail current of the IGBT.

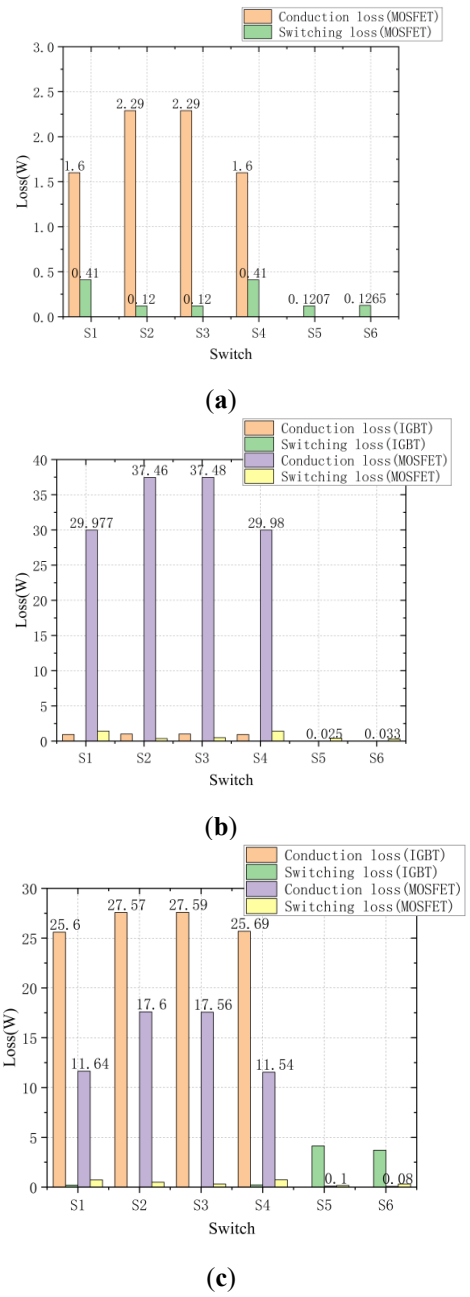


Figure 13. Loss analysis of the three-stage scheme under different load conditions. (**a**) Light load. (**b**) Medium load. (**c**) Heavy load.

When the load current increases to 100 A, the losses of the devices are illustrated in Figure 13c. In this case, all three stages are utilized, as illustrated in Figure 5a. The IGBTs are active during the high-current period; hence, for all six switch sets, the IGBT conduction loss becomes dominant. Under the high-load-current condition, the total losses of both approaches have increased, but the proposed method is still more efficient than the Mode 1 scheme, as its total loss is 174.69 W, which is lower than 182.5 W of the Mode 1 scheme. Based on the above results, PD-PWM with the three-stage control scheme is selected as the optimal control strategy for the ANPC converter in the cost analysis that follows, where it will be used to identify the best switch configuration.

The proposed method differs from previously reported hybrid Si/SiC approaches in both control scope and optimization objective. The current-dependent switching strategy in [10] is primarily designed for device-level switching-loss reduction, whereas the hybrid ANPC configuration in [11] improves converter efficiency but does not jointly consider load-dependent device operation and lifecycle cost. Our previous

ANPC loss analysis in [19] examined the influence of device technology and PWM schemes; the present work extends this by integrating a three-stage current-dependent switching strategy with a CSF-based semiconductor configuration method. Since the reported studies employ different semiconductor devices, power ratings, switching frequencies, and operating conditions, a direct numerical cross-study loss comparison would not yield a fair assessment. Accordingly, the present comparison focuses on the differences in control functionality and optimization objectives.

4.3. Practical Implementation Considerations

The present study is based on detailed PLECS simulations using manufacturer-provided device characteristics, and experimental validation is not included in the current work. In practical implementation, several issues should be considered. First, accurate current sensing is required for reliable detection of the two transition thresholds I_1 and I_2. A small hysteresis band around these thresholds can be introduced to avoid frequent mode transitions caused by measurement noise. Second, the relative turn-on and turn-off delays between the SiC MOSFET and Si IGBT must be implemented using gate drivers with sufficiently small propagation-delay mismatch. Since the selected delays are t_1 = 0.2 μs and t_2 = 0.6 μs, device and driver tolerances should be considered when determining the practical timing margins.

In addition, parasitic inductance, unequal gate-loop impedance, and device-parameter variations may result in transient current imbalance, voltage overshoot, and increased EMI in the parallel branches. Symmetrical power-loop layouts, Kelvin-source connections, appropriate gate-resistance tuning, and, where necessary, snubber or damping networks are therefore important for hardware implementation. Thermal coupling between the Si IGBT and the SiC MOSFET may also modify their conduction characteristics, thereby shifting the effective current-sharing boundaries. Future work will therefore include double-pulse characterization of the hybrid switch set and converter-level experiments under light-, medium-, and heavy-load conditions to validate the predicted loss reduction and switching-mode transitions.

The real-time computational burden of the proposed three-stage strategy is low. The online implementation requires only measuring the instantaneous current, comparing it with the two predefined thresholds I_1 and I_2, and selecting among three predefined switching patterns. No iterative optimization or online solution of the loss model or CSF is required, because the CSF-based semiconductor configuration is determined offline during the converter design stage.

For the 10 kHz switching frequency used in this study, the PWM period is 100 μs, leaving sufficient time for current measurement, threshold comparison, and mode selection in a conventional digital controller. The sub-microsecond relative gate delays t_1 and t_2, however, should preferably be generated by dedicated PWM peripherals, FPGA logic, or appropriately designed gate-driver circuits to ensure deterministic timing. Thus, the proposed control structure is compatible with practical DSP/FPGA-based converter controllers without introducing significant online computational complexity.

5. Optimal Combination of Hybrid Switch Sets and Single Switches for the ANPC Converter

Although the parallel hybrid Si/SiC switch set is beneficial in terms of reducing the total power losses, the cost per ampere ($/A) of WBG devices remains significantly higher than that of Si-based devices. Using the PD-PWM scheme, some devices suffer less stress than others in the same leg. For example, switches S_{a1}, S_{a4}, S_{a5}, and S_{a6} are normally either off or on during a sinusoidal cycle, hence they experience less stress than the other two switches. Leveraging this, an ANPC with an optimal mix of hybrid switch sets and single switches can be designed, providing the best trade-off between losses and cost while maintaining high power capability. To evaluate the performance of the final design, a CSF is defined as an indicator for quantifying the total lifecycle cost of the system using hybrid parallel switch sets. It incorporates both the

initial procurement expenditure and the operating cost arising from power losses of the designed converter, which increase with device aging and prolonged operation. The CSF is given as:

$$CSF = (P_{Schemei} - P_{Scheme2})T_W T_L R_E/1000 + Cost \tag{15}$$

where T_W is the average working time per day for an ANPC based off-board EV charger which is set to 14 h corresponding to the average working period of a car park [24]; T_L is the average lifetime of a semiconductor power switch which is significantly influenced by the switching frequency, power cycle, operating temperature and it is about 21,650 h (4.24 years) on average [25]; R_E is the average electricity tariff, which is given as 0.24 $/kWh; $P_{Scheme2}$ is the total power loss of the topology using high-current-rated SiC MOSFETs only [26]; $P_{Schemei}$ denotes the loss of the i-th scheme and can be expressed as:

$$P_{Schemei} = \frac{P_0 + K_D D}{1 - K_T R_\theta \ （1 + \lambda D）} \tag{16}$$

where P_0 denotes the total loss at the reference junction temperature; λ is the relative gain coefficient of thermal resistance, set to 0.2; R_θ represents the device's initial thermal resistance (see Table 3), and $D(t)$ accounts for the accumulated damage, expressed as:

$$D(t) = min\{t/T_L, \quad 1\} \tag{17}$$

where K_T, K_D are the temperature-sensitivity gain and aging-sensitivity gain, respectively. Each is formed by a linear combination of the corresponding temperature/aging coefficient and the reference power [27], expressed as:

$$K_T = \beta_{\text{cond}} P_{\text{cond}} + \beta_{\text{sw}} P_{\text{sw}} \tag{18}$$

$$K_D = k_{\text{cond}} P_{\text{cond}} + k_{\text{sw}} P_{\text{sw}} \tag{19}$$

where k_{cond} and k_{sw} are the conduction and switching aging factors, which are set to 0.1 and 0.03, respectively; P_{cond}, P_{sw} denote the device's conduction and switching losses, and β_{cond} and β_{sw} are the conduction and switching temperature coefficients, respectively. For MOSFETs and IGBTs, they are given by:

$$\beta_{\text{condMOS}} = \frac{R_{DS\_25°C}/R_{DS\_175°C} - 1}{150} \tag{20}$$

$$\beta_{\text{condIGBT}} = \frac{V_{CE\_25°C}/V_{CE\_175°C} - 1}{150} \tag{21}$$

The switching temperature coefficient can be calculated as:

$$\beta_{\text{sw}} = \frac{E_{SW\_25°C}/E_{SW\_175°C} - 1}{150} \tag{22}$$

where $R_{DS\_25°C}$, $R_{DS\_175°C}$, $V_{CE\_25°C}$, $V_{CE\_175°C}$, $E_{SW\_25°C}$ and $E_{SW\_175°C}$ denote, respectively, the device's on-state resistance, saturation voltage, and switching energy loss measured at 25 °C and 175 °C. The parameters for the devices used in the case study are listed in Table 4.

Table 4. Parameters of the CSF for different devices.

Devices	β_{cond} (°C^{-1})	β_{sw} (°C^{-1})
C3M0025065K	2.13×10^{-3}	2×10^{-3}
C3M0015065K	2.22×10^{-3}	2×10^{-3}
IKQ120N60TXKASA	1.78×10^{-3}	3.77×10^{-3}

Taking the loss distribution and the cost into account, five configurations that use mixed parallel Si IGBT/SiC MOSFET and single IGBTs are designed, their respective losses and costs (in terms of switching devices only) are evaluated, and the results are summarized in Table 5 together with the first three schemes

having switches of uniform device type. For all the hybrid configurations listed in the table, only the switches mentioned are replaced by single switches. All other switches in a phase leg use the parallel hybrid SiC+Si switch sets. It is shown that when all switches are high-current-rated SiC devices (Scheme 2), the overall loss is 162.4 W. The total cost is $352.44, and the CSF is $352.44 (Conventional scheme using C3M0015065K, $58.74). In contrast, when Si switches are used only (Scheme 1), the configuration has a total power loss of 200.18 W, with a significantly reduced cost of $84.06, and the CSF is $282.11 (Conventional scheme using IKQ120N60TXKASA $14.01) [14]. As can be seen in Table 5, Scheme 7 offers the best trade-off between loss and cost with an overall loss of approximately 176.13 W, achieving a 12.02% loss reduction compared to the single-Si-switch topology. The cost required in this scheme is $118.36, only 33.58% of the conventional all single SiC MOSFETs structure. Besides, its CSF is the minimum one among all five hybrid configurations at only $179.29, achieving a 22.46% reduction compared with the topology using only parallel hybrid switch sets. As a result, Scheme 7 achieves the optimal performance compared with all other topologies. The chosen structure is illustrated in Figure 14.

Table 5. Loss and cost analysis of different hybrid switch configurations.

Number	Hybrid Structure	Conduction Loss (W)	Switching Loss (W)	P_0 (W)	Cost ($)	CSF ($)
1	All switches with IGBT	168.76	31.42	200.18	84.06	282.11
2	All switches with MOSFET	155.83	6.57	162.4	352.44	352.44
3	All switches with parallel switch sets	165.59	9.1	174.69	177.54	231.22
4	Switches S_{a5}, S_{a6} with MOSFET	166.58	11.34	177.92	149.52	221.35
5	Switches S_{a5}, S_{a6} with IGBT	165.62	22.94	188.56	146.38	275.58
6	Switches S_{a1}, S_{a4} with IGBT	162.36	10.39	172.75	146.38	188.14
7	Switches S_{a5}, S_{a6} with MOSFET; switches S_{a1}, S_{a4} with IGBT	164.80	11.33	176.13	118.36	179.29
8	Switches S_{a1}, S_{a4}, S_{a5}, S_{a6} with IGBT	162.87	24.94	187.81	115.22	240.56

According to Figure 5a and Equations (4) and (7), during the positive half-cycle of a sinusoidal period, particularly in the third stage with a high output current, S_{a1} and S_{a2} operate with a large PWM duty ratio, so conduction losses dominate in this interval. By contrast, the neutral-point clamping switch S_{a5} runs with a small duty ratio, making switching losses predominant in this device. For the negative half-cycle, the losses of S_{a6} are dominated by switching losses. Consequently, replacing S_{a5} and S_{a6} with fast-switching devices is advantageous for further reducing total losses.

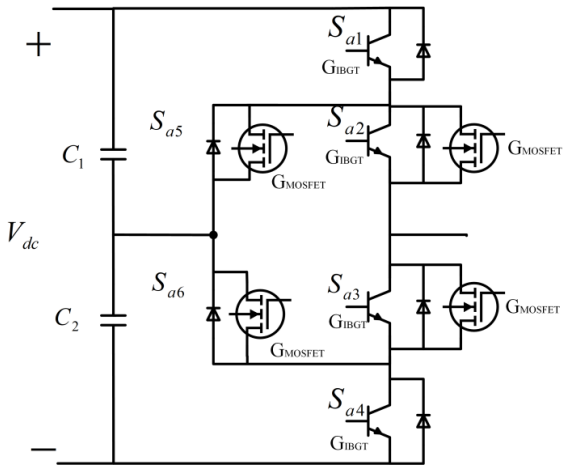


Figure 14. Optimal combination of parallel hybrid switch-sets and single switches in an ANPC phase leg.

Figure 15 shows the evolution of CSF for all schemes over their operation lifetime. Taking Scheme 2 as the baseline, its CSF remains constant. Overall, the CSF of each topology increases with service life. Notably, up to 5 years, Scheme 7 achieves the lowest CSF, indicating a superior cost–efficiency trade-off. At 4.24 years (approximately 21,650 h), its CSF is \$179.29.

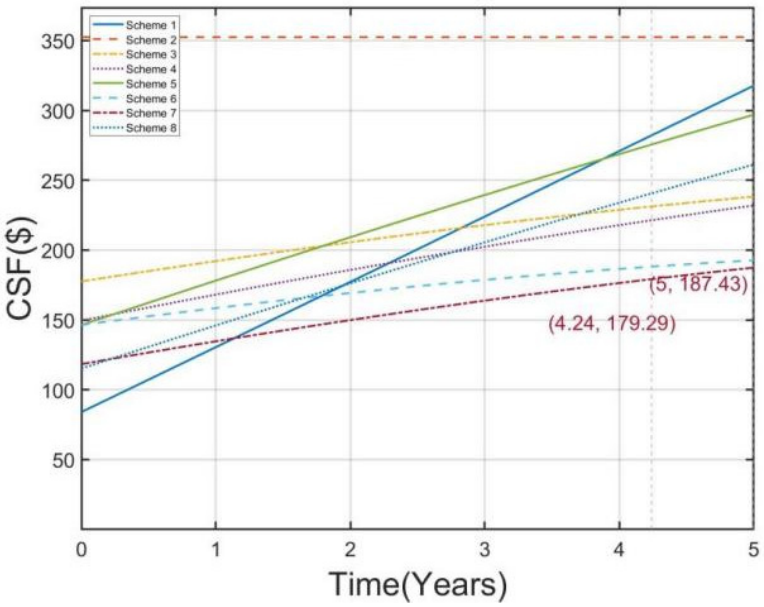


Figure 15. Variation of CSF with operating time for the eight switch-configuration schemes.

5.1. Sensitivity of the Cost-Saving Function

The CSF depends on economic and operating assumptions, particularly the electricity tariff and cumulative operating time. To evaluate the robustness of the identified optimal configuration, a sensitivity analysis is first performed with respect to the electricity tariff while retaining the remaining parameters at their base-case values. The tariff is varied from 0.12 to 0.36 \$/kWh, covering ±50% of the nominal value of 0.24 \$/kWh.

Under the nominal tariff, Scheme 7 yields the minimum CSF of \$179.29. It also remains the preferred configuration at 0.12 \$/kWh, with a CSF of \$148.82. However, at 0.36 \$/kWh, Scheme 6 becomes marginally more economical, with a CSF of \$209.02 compared with \$209.75 for Scheme 7. This shift occurs because the higher electricity tariff increases the weighting of power loss relative to the initial semiconductor cost. Therefore, Scheme 7 provides the best efficiency–cost compromise under the base operating scenario, whereas configurations with lower losses may become preferable in regions with substantially higher electricity prices.

The influence of lifetime can also be observed from Figure 15. As cumulative operating time increases, the loss-related component of the CSF becomes increasingly important. Scheme 7 maintains the lowest CSF over the investigated service interval up to approximately 5 years under the nominal tariff. Changes in daily utilization have a similar effect because they alter the cumulative operating hours over a fixed calendar period. Consequently, the proposed CSF should be regarded as a configurable design tool: the tariff, operating profile, and expected service life can be adjusted for a particular charging station before determining the preferred semiconductor configuration.

5.2. Thermal and Reliability Considerations

Although the CSF incorporates temperature- and aging-dependent variations in device losses, the configuration study is based primarily on nominal device parameters. In long-term operation, repetitive

junction-temperature cycling may lead to degradation of semiconductor packaging and interconnections, while variations in R_{DS}(on), V_{CE}(sat), threshold voltage, and switching energy can progressively alter the loss distribution between the SiC MOSFET and Si IGBT. These effects may modify both current sharing and the effective switching boundaries of the hybrid switch set.

Parameter mismatch is particularly important for parallel hybrid devices. Differences in gate resistance, driver propagation delay, package and busbar inductance, and temperature-dependent conduction characteristics can lead to unequal transient current sharing. The proposed three-stage strategy reduces the exposure of the lower-current-rated SiC MOSFET to severe high-current conditions by transferring operation to the IGBT when the current exceeds I_2. Nevertheless, practical designs should determine I_1 and I_2 using worst-case device tolerances and junction-temperature conditions rather than nominal characteristics alone. Adequate heatsink design, low and symmetrical parasitic inductance, and sufficient junction-temperature margin are therefore required to preserve the expected efficiency and reliability benefits over the converter lifetime.

6. Conclusions

This paper investigates a three-level ANPC converter using hybrid Si IGBT/SiC MOSFET parallel switches for high-power off-board EV charging. A three-stage switching scheme was proposed to exploit the complementary characteristics of Si and SiC devices across a wide load range while avoiding excessive SiC current stress. Compared with conventional Mode 1 operation, the proposed strategy reduces the total loss by 2.85% at 50 A and 4.28% at 100 A. A cost-saving function (CSF) was further introduced to jointly consider semiconductor procurement cost and loss-related operating cost. Under the base-case assumptions, Configuration 7 reduces the total converter loss by 12.02% relative to the all-Si configuration and reduces the semiconductor cost by 66.42% relative to the all-SiC configuration, while achieving the minimum CSF of $179.29. Sensitivity analysis further indicates that the optimal configuration is contingent on both the electricity tariff and operating conditions, confirming that the proposed CSF can serve as a versatile design tool adaptable to different charging scenarios. Future work will focus on experimental validation of the hybrid switch set and converter, including transient current sharing, parasitic effects, thermal behavior, and long-term device reliability.

Author Contributions

Conceptualization, Y.Z. and K.L.; Methodology, Y.Z.; Software, Y.Z.; Validation, Y.Z.; Formal Analysis, Y.Z.; Investigation, Y.Z.; Resources, K.L. and L.Z.; Data Curation, Y.Z.; Writing—Original Draft Preparation, Y.Z.; Writing—Review and Editing, K.L. and L.Z.; Visualization, Y.Z.; Supervision, K.L. and L.Z.; Project Administration, K.L.; Funding Acquisition, K.L. All authors have read and agreed to the published version of the manuscript.

Ethics Statement

Not applicable.

Informed Consent Statement

Not applicable.

Data Availability Statement

The data supporting the findings of this study are available from the corresponding author upon reasonable request.

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Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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